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Design of Low Phase Drift CMOS Frequency Synthesisers

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Design of Low Phase Drift CMOS Frequency Synthesizers

Cyril Lahuec
Design of Low Phase Drift
CMOS Frequency Synthesisers

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Submitted in partial fulfilment for the
Degree
Doctor of Philosophy

Cork Institute of Technology
Department of Electronics Engineering

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Abstract

This thesis presents a methodology for the development of high performance video clock synthesisers that have high (2000) input to output clock multiplication ratios. The synthesisers are required to be compatible with standard CMOS technologies and they must exhibit very low drift between their input and output clocks.

The methodology used borrows techniques established for RF synthesisers in the GHz range. In the RF domain there are significant constraints on spectral spread and because of this there has been significant interest in phase noise generated by intrinsic device noise. Simple and accurate models were developed that help understand the up and down conversion of this device noise into phase noise. Using these ideas all possible sources of noise in the video synthesiser were studied and optimised. A key result of this analysis was a redesign of the bias circuitry leading in itself to a performance improvement of a factor of eight over a conventional bias scheme.

In RF applications there is usually a small multiplication ratio between input and output clocks. The bandwidths of the synthesiser loops are beyond the 1/f noise corner of the oscillators making the 1/f noise in the oscillator less important. The challenge with video clock synthesisers is that there is a large multiplication ratio and a low bandwidth requirement so this makes the 1/f noise in the synthesiser important. The 1/f noise causes a significant drift between input and output clocks. This drift is particularly relevant for video clocks that determine the sampling instants of the analogue video signal. The drift in these clocks leads to erroneous or missing video samples which causes bad or lost pixels in a displayed image.

The clock synthesiser described in this thesis performed frequency multiplication of an input clock ranging from 15kHz to 5MHz with a programmable multiplication ratio of 4 to 1024. The circuit was implemented on a chip using a commercial 0.25μm CMOS process. A sample of measured drift in the optimised device is 0.42ns for a 48kHz reference and a multiplication ratio of 584. These measured drift results represent the lowest reported to date.
Remerciements

Toujours délicat de ne froisser personne pour cette page. Les gens dont le nom apparaît se sentent sans doute content tandis que ceux qui ne figurent pas dans la Liste me traiteront sans doute d’ingrat.

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Petra a lavar ar gwenan?

Evit dastum, kemer poan.
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1.0 Introduction.

The thesis introduces a methodology for the development of high performance video clock synthesers. A key requirement of these clocks is that there is very low drift between the input and output clock. To achieve this, the thesis introduces a new architecture which minimises the re-circulation of phase noise. It also borrows techniques used in the design of RF synthesers which allows for the estimation and subsequent reduction of phase noise in the syntheser.

The following presents a review of video signals and sampling to put the research in context and then the organisation of the thesis is discussed.

1.1 Video signal and TV screen.

In most TV sets, the device used to display the image is known as the Cathode Ray Tube (CRT). It uses an electron gun to excite phosphorous dots on the screen. The phosphor dots emit light once hit by the electron beam. The electron gun is controlled by a signal, which contains the necessary information to display the image. This signal is called the video signal. This is an analogue signal, an example of which is shown on figure 1.1. A video signal is composed of a number of different signals. The first signal contains timing information and is known as the horizontal synchronisation signal. It consists of rectangular pulses which define the beginning and the end of a line on the screen. The
frequency of these pulses changes with the video standard being used but it is typically under 300kHz. For conventional video it is 15.7kHz while SXVGA computer monitors require these pulses at frequencies up to 150kHz [1]. The video signal between the two pulses contains the information used to draw one line on the screen. This is referred to as the active video line. It defines the brightness of the individual dots or pixels along the line being drawn. This is all that is required for a black and white TV and together the pulses and the video information are known as the composite video signal [2]. A colour TV signal has an additional signal called the colour burst. This is found just after the synchronisation pulse. In all TV sets there is a decoder which takes in the composite video signal and converts this to three signals which drive three electron guns: a red, a green and a blue gun.

![Video signal, synchronisation pulse and active video line.](image)

A serious draw back of CRTs is that over a certain size, they become very heavy and power hungry. Another type of screen that overcomes these has recently been introduced on the market. This is called the flat screen. The main drive behind the development of the flat screen was probably the development of battery powered portable computers. CRTs were not suitable for this market because of power they require to operate. The first flat monitors were small (12-13 inch) and had a relatively low resolution due to a low number of pixels per line. Progress has been made in the last couple of years to produce large high quality flat screens and they are now commonly in use as
TV screens. The screen used in laptop computers is referred to as Liquid Crystal Display (LCD) while TVs use Plasma Display Panel (PDP) technology. The advantages of Plasma displays is that panels up to 80 inches wide by only 4 inches thick can be constructed.

Flat screens are also technologically more complex than CRTs to build and as a result are much more expensive. In a PDP the screen is made up of a matrix of cells receiving a constant flow of low-pressure gas (neon or xenon). This matrix is placed between two sheets of glass. The glass is covered with electrodes which control the excitation of the gas in the cells. A particular pixel can be individually addressed using row and column electrodes. The rows and columns are connected to circuits that control when a charge is applied to a particular pixel. Depending on the amount of charge, the emission of light will be more or less strong which allows control on the hue. Just like in a CRT, the pixels are composed of three parts, one for each colour. In summary, unlike in CRT where a scanning electron beam draws the picture line by line, in a flat screen each pixel receives its own signals. This requires sampling and digitising the video information and the resulting digital words are individually sent to the corresponding pixel with the proper timing. This implies an analogue to digital conversion of the three video signals at instants defined with respect to the horizontal synchronisation, figure 1.2.

Figure 1.2: Digitising video signal
1.2 Sampling video signals.

A clock signal is generated from the horizontal synchronisation signal using a frequency synthesiser, this clock is called the pixel clock. At the first edge of the pixel clock, the video signals Red, Green and Blue (RBG) are sampled. The result of the conversion is sent to the first pixel of the screen and this is repeated along the video line signal to generate the digital words for the pixels along the line. From this it is clear that the generated pixel clock must have as many cycles, between two synchronisation pulses, as the number of pixels on a screen line. More importantly, for the pixel to receive the correct data at the correct instant, the pixel clock must be very stable in time. To generate the pixel clock signal, a frequency-locked oscillator is used. The phase of this oscillator receives periodical updates from the horizontal synchronisation pulse. This allows the pixel clock to stay phase-aligned with the horizontal sync pulse. The synchronisation pulse occurs at a low frequency (between 32kHz and 220kHz) from which a large number of clock edges must be generated to sample the video signal. A sample system might have a horizontal synchronisation signal of 32kHz and a corresponding pixel clock of 32.768MHz. This system has 1024 pixels per line (1024 x 32kHz=32.768MHz). In this system the oscillator is running for 31.5µs without a phase update. This time is long enough to allow the edges in the oscillator to drift away from their ideal positions. This drift is caused by the inherent noise sources in the synthesiser causing phase movement of the clock or phase noise. In other words, the last pixels on the line will sample the video line at incorrect points. When the drift is sufficiently large it will cause pixels to have data corresponding to pixels which are ahead or behind it in the pixel row. This situation is depicted on figure 1.3 where the last pixel being sampled (red dot) gets the information for the first pixel of the next line.
To illustrate typical drift in an oscillator some sample drift measurements are shown. The results are taken from a typical oscillator configuration the Phase locked loop (PLL). The data is taken from a PLL designed for on a 0.25μm CMOS process. The input frequency is set at 100kHz and the multiplication ratio between input and output signals is 256 giving an output frequency of 25.6MHz. Using a WAVECREST DTS2077 [3], the time uncertainty between an edge of the reference and the 256th edge of the output clock is measured. The results are shown on figure 1.4. The peak to peak deviation is 8.78ns or 22.5% of the clock cycle. The PLL performs reasonably well but once this peak-to-peak deviation is put in the context of a 100MHz clock it represents almost one complete cycle. The reason the drift is so significant in this PLL is that there are significant low frequency noise components in CMOS [4]. A solution to this could be to use of a bipolar process instead of a CMOS process since bipolar transistors have very low 1/f noise [5]. CMOS is far more desirable because of the lower cost of the process. It was also shown in [6], that under certain design conditions, CMOS oscillators can perform well in terms of noise and thus it was a reasonable goal of this thesis to design such an oscillator in CMOS.
When designing such a structure, the next consideration beyond the choice of process is the architecture. PLLs and DLLs are considered as possible architectures in this thesis. Finally a hybrid circuit called the factorial DLL [7] [8], FDLL, is presented as a worthwhile possibility.

With the architecture decided, the next step involved gaining a good understanding of the causes of, and models for, the noise in an oscillator. With this understanding, components of the oscillator are optimised to improve the overall noise and thus the drift in the oscillator.

1.3 Thesis organisation.

Chapter 2 gives theoretical background on noise in an oscillator. A suitable noise model is explained and the main equations describing it are introduced. Frequency synthesisers such as Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs) are introduced. Their building blocks are briefly explained before concentrating on their behaviour in the presence of noise.
In chapter 3, different CMOS ring oscillators are examined. The motivation for this is to compare the potential drift in each topology. The topologies investigated are the current-starved inverter oscillator (CSO), a single-ended inverter chain with variable capacitors and a fully differential inverter chain with delay control. The phase noise model presented in chapter 2 is used to study the noise behaviour of these different ring structures. The topologies were also tested for their ability to withstand deterministic sources of noise and these results are reported.

In chapter 4 the Fractional Delay-Locked Loop synthesiser is explained. The design of such a circuit is shown in detail. Identification of major sources of low frequency noise is identified and the topology is optimised to reduce the overall drift.

Different versions of the FDLL were implemented on chip to verify theory and chapter 5 shows the practical results obtained from the chip designed in chapter 4. Measurements of phase noise are compared to the prediction from theory in chapter 4. The drift was also measured and compared with predictions in chapter 4.

Chapter 6 concludes the thesis.

1.4 References.


CHAPTER 2

Background theory on phase noise, PLLs and DLLs

2.0 Introduction.

This chapter introduces a number of equations and terms that are used throughout the thesis. These equations cover integrated circuit (IC) device noise and its conversion to phase noise in oscillators. It also introduces measurement of phase noise and how PLL and DLL closed loops modify VCO phase noise.

It begins by investigating the spectral distribution of a phase noise modulated signal. This is done by manipulating a sinusoidal signal, in which the phase noise is modelled by a sinusoid of known amplitude and frequency. The equations that result allow the introduction of phase noise measurement and simple relationships to relate measured spectral noise distributions and phase noise.

With this understanding of phase noise the spectrum of an actual oscillator is then shown and its characteristics are discussed in the context of the simple case of phase modulation by a deterministic signal. This is followed by introducing a suitable phase noise model along with a method of estimating its parameters from the IC devices in the oscillators.

With the phase noise of the open loop oscillator described the next sections look at the impact of putting the oscillators into Phase-Locked Loops and Delay-Locked Loops. Along with a brief explanation of these circuits, equations are quoted that provide insights into the effects of noise on these circuits. All noise sources including the phase noise of the oscillator are considered.
2.1 Phase noise.

2.1.1 Noise.

Noise is defined as any unwanted disturbance to a signal. If noise is caused by interference from another signal the disturbance is usually deterministic. Variations in the power supply voltage or coupling between two signal lines are examples of deterministic noise. They usually appear as periodic disturbances and are seen as spectral components on a spectrum analyser. Other types of fluctuations are random and are due to intrinsic device phenomena such as thermal noise or 1/f noise (also called flicker noise). These noise sources are distributed over the frequency spectrum. Thermal noise has constant amplitude over frequency (white spectrum) while the amplitude of 1/f noise is inversely proportional to the frequency. When these noise sources affect the phase of a signal they result in phase noise. Typically phase noise will exhibit both deterministic and random noise.

In order to study how noise affects a signal, the next section looks at a signal which has its amplitude and phase modulated by a known signal. The results will be generalised to any disturbances.

2.1.2 Modulated signal.

In a general way, a signal can be expressed as \[1\]:

\[
V(t) = [A + a(t)]\sin[\omega_0 t + \phi_m(t)]
\]

A : amplitude.
a(t) : amplitude noise.
\(\omega_0\) : nominal angular frequency.
\(\phi_m(t)\): phase modulation.

(2.1)

Figure 2.1 shows a sinusoidal signal that has been affected by different kinds of noise. Figure 2.1(a) shows the signal with white amplitude noise. Figure 2.1(b)
shows the signal with white phase noise. Figure 2.1(c) shows a signal affected by both types of noise and figure 2.1(d) shows a signal with 1/f phase noise.

Figure 2.1: Time domain representation of a sinusoidal signal with (a) white amplitude noise, (b) white phase noise, (c) white amplitude and white phase noises, (d) 1/f phase noise.

Amplitude noise and phase noise can contribute to the total noise power. Because practical oscillators have a mechanism which limits the amplitude of oscillation, the amplitude noise is generally considered negligible [2], [3]. Therefore, most of the noise power is due to phase noise, so equation (2.1) can be rewritten as:

$$V(t) = A \sin[\omega_n t + \phi_n(t)]$$  \hspace{1cm} [V]  \hspace{1cm} (2.2)

In order to examine the spectral content of such a signal, a known phase modulation \(\phi_n(t)\) is used to modulate the frequency of \(V(t)\) (equation (2.2)). \(\phi_n(t)\) is a sinusoidal signal of amplitude \(m\) radians and with angular frequency \(\omega_n\):
\[ V(t) = A \sin[\omega_0 t + m \sin(\omega_m t)] \]  

Equation (2.3) can be expanded using Bessel functions [4]:

\[ V(t) = A \sum_{n=-\infty}^{\infty} J_n(m) \sin[(\omega_0 + \omega_m) t] \]  

This equation shows that the spectrum will contain an infinite number of spectral components at frequencies \( f_0-nf_m, \ldots, f_0-2f_m, f_0-f_m, f_0, f_0+f_m, f_0+2f_m, \ldots f_0+nf_m \) with amplitudes defined by the Bessel's coefficient \( J_n(m) \). Fortunately, only a small number of these coefficients are significant. For example, if \( m=0.2 \) then the second Bessel coefficient \( J_2(m) \) equals 0.005. This simply leaves \( J_0 \) and \( J_1 \), the other rays can be ignored [5]. Moreover, if the modulation index satisfies \( m \ll 1 \) then \( J_0=1 \) and \( J_1=m/2 \). The spectrum is then composed of three components: one corresponding to the carrier and two side components. This is equivalent to the narrow band model [6]. This model uses the fact that the phase disturbance is very small compared to the nominal angular frequency for a practical oscillator. This allows simplifications and the spectrum can be obtained by developing equation (2.3) and using simple trigonometry. These steps are described by the following equations.

Equation (2.3) can be rewritten as:

\[ V(t) = A \sin(\omega_0 t) \cos[m \sin(\omega_m t)] + A \cos(\omega_0 t) \sin[m \sin(\omega_m t)] \]  

Considering \( m \sin(\omega_m t) \ll 1 \), equation (2.5) simplifies to:

\[ V(t) = A \sin(\omega_0 t) + A m \cos(\omega_0 t) \sin(\omega_m t) \]  

After further steps, equation (2.6) leads to:

\[ V(t) = A \sin(\omega_0 t) + \frac{Am}{2} \sin[(\omega_0 + \omega_m) t] - \frac{Am}{2} \sin[(\omega_0 - \omega_m) t] \]  

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This is equivalent to developing equation (2.4) using only coefficients $J_0$ and $J_1$. Equation (2.7) shows that the phase disturbance $m \sin(\omega_m t)$ gives rise to two sinusoidal perturbations with amplitude $A_m/2$ at frequencies $f_0 - f_m$ and $f_0 + f_m$. The amplitude spectrum is then composed of a spectral component with amplitude $A$ at frequency $f_0$ and two side components with amplitude $A_m/2$ at frequencies $f_0 - f_m$ and $f_0 + f_m$. The amplitude spectrum is shown on figure 2.2(a).

The power spectrum plots the rms power dissipated in a $1\Omega$ resistor versus the frequency at which the power is dissipated. The rms voltage of a sine wave is defined as the equivalent dc voltage which would dissipate the same energy over a cycle, thus:

$$V_{\text{rms}} = \sqrt{\frac{1}{T} \int_{0}^{T} [A \sin(\omega_0 t)]^2 \, dt} \quad [\text{V}] \quad (2.8)$$

$$= \sqrt{\frac{A^2}{2}}$$

Therefore to compute the rms voltage of a sinusoid, its amplitude is divided by $\sqrt{2}$. The power spectrum of the signal defined by equation (2.7) is simply deduced from the amplitude of the three sinusoids. The power spectrum, denoted $S_v(f)$, is composed of three rays with power $(A/\sqrt{2})^2 = A^2/2$ at frequency $f_0$ and two side rays with power $(A_m/\sqrt{2})^2 = A^2m^2/8$ at frequencies $f_0 - f_m$ and $f_0 + f_m$. This power spectrum is shown on figure 2.2(b).

### 2.1.3 Measurement of phase noise.

In the previous section the power spectrum $S_v(f)$ of the phase-modulated signal $V(t)$ defined by equation (2.7) was obtained. This power spectrum which is shown on figure 2.2(b) can be measured using a spectrum analyser. A related quantity $S_\phi(f)$ is a measure of the power in the sidebands relative to the power
of the carrier. For the signal described by equation (2.7), the rms power of one sideband is $A^2m^2/8$, thus the rms power of both sidebands is $A^2m^2/4$.

![Amplitude vs. Frequency](image1)

![Power Spectrum](image2)

Figure 2.2: Frequency modulated signal spectrum, (a) amplitude spectrum (b) and power spectrum.

Normalising this to the carrier power: $(A^2m^2/4) / (A^2/2)$ gives $m^2/2$. This gives a direct mechanism for quantifying the impact of a spectral ray in the frequency domain on the time domain phase variation. That is, measuring the power in the ray relative to the carrier gives a direct calculation of $m^2/2$ and thus $m$, which is used in the time domain equation (2.3). Another quantity which is sometimes used is called $L(f)$. This is the phase noise in a single sideband. In the general case, the sideband power is calculated over a 1Hz bandwidth, thus $L(f)$ is defined as [7]:

$$L(f) = \frac{P_{\text{sideband}}(f_0 + f_m, 1\text{Hz})}{P_{\text{carrier}}}$$  \hspace{1cm} (2.9)

From the above discussion there is a simple relation between $L(f)$ and $S_\phi(f)$ [7]:

$$L(f) = \frac{S_\phi(f)}{2}$$  \hspace{1cm} (2.10)
Obtaining the power spectrum $S_v(f)$, as on a spectrum analyser, also gives the phase noise spectrum $S_\phi(f)$ from the measurement of the relative power of the sideband to the carrier power.

$L(f)$ and $S_\phi(f)$ are usually plotted on a diagram where the carrier power is omitted and the x-axis represents the offset from the carrier frequency $f_0$ rather than frequency [3]. Figure 2.3 shows the relation between the power spectrum of the signal (as seen on a spectrum analyser) $S_v(f)$ (figure 2.3(a)), the phase noise spectrum (the quantity of interest) $S_\phi(f)$ (figure 2.3(b)) and the commonly used phase noise measurement $L(f)$ (figure 2.3(c)).

Usually $L(f)$ is expressed in decibel relative to the carrier at a given frequency offset:

$$L_{\text{dBc}}(f) = 10\log[L(f)]$$

$[\text{dBc}/\text{Hz}] \quad (2.11)$

$L(f)$ will be used instead of $L_{\text{dBc}}(f)$ to simplify notation. A reading in $L(f)$ is always given for a specific offset from the carrier frequency such, for example, -120dBc at an offset of 100kHz.

Figure 2.3: measure of phase noise, (a) power spectrum $S_v$, (b) phase noise spectrum and (c) $L(f)$.
2.1.4 Phase noise spectrum of an oscillator.

The simple example of a sinusoid phase modulated by another sinusoid is interesting in understanding how phase noise translates into spectral power. However, an oscillator has its phase modulated by random signals rather than known signals. The power of the signal is not located at fixed frequencies but tends to spread over a bandwidth around the centre frequency. The spectrum will not look like the one depicted on figure 2.3 but will look more like the one shown on figure 2.4.

Usually the spectrum analyzer displays $L(f)$ (or $S(f)$) in dBC on a semi-log plot as shown on figure 2.6. In this case the x-axis is the frequency offset from the carrier. This representation allows for noise identification. To understand how it is identified, it is necessary to define the transfer function of an oscillator and explain how it shapes its own noise.

A voltage-controlled oscillator in its simplified form is basically a linear system, which outputs a frequency $f$ for given input voltage $V_{in}$. This is represented on figure 2.5; the slope of the line gives the gain of the oscillator, $K_{VCO}$, in Hz/V.

\[ f = K_{VCO}V_{in}(t) \quad \text{[Hz]} \quad (2.12) \]

Phase is the integral of frequency:

\[ \phi(t) = 2\pi \int f \, dt \]
\[ = 2\pi \int K_{VCO}V_{in}(t) \, dt \quad (2.13) \]

Equation (2.13) shows that to produce phase an oscillator integrates its input voltage. This is represented in the frequency domain by a system with a transfer function:

\[ H_{VCO}(f) = \frac{K_{VCO}}{2\pi f} \quad (2.14) \]
Figure 2.4: Actual oscillator’s spectrum. The power of the sideband at an offset $f_m$ from the carrier is evaluated for a 1Hz bandwidth.

In the frequency domain, the response of the oscillator to an input voltage $V_{in}$ is given by:

$$K_f = V(f)H_{vco}(f)$$  \hspace{1cm} (2.15)$$

Where $V(f)$ and $H_{vco}(f)$ are the Fourier transforms of the output phase and the input voltage. By definition [6], [8] the relationship between the output and input power spectrum ($S_{out}(f)$ and $S_{in}(f)$) of a system with transfer function $H(f)$ is given by:

$$S_{out}(f) = V_{in}(f)H_{vco}(f)$$

Figure 2.5: VCO characteristic.
Random phase noise has two different origins. 1/f noise, which is dominant at low frequencies and thermal (white) noise which has a constant amplitude throughout the spectrum. If $S_{in}(f)$ represents the noise power spectrum of a white noise voltage then $S_{in}(f)$ is constant. Applying equation (2.16) with $H(f)$ given by equation (2.14) in this case will result in a phase spectrum which varies with $1/f^2$. In a semi-log plot, $S_{out}(f)$ will then roll off with a slope of $-20$dB/decade due to the following calculation:

$$10 \log_{10} \left( \frac{1}{f^2} \right) = 10 \log_{10} \left( \frac{1}{1} \right) - 10 \log_{10} \left( f^2 \right) = -20 \log_{10} (f)$$  \hspace{1cm} (2.17)

In the same way, if $S_{in}(f)$ represents the noise power spectrum which varies as $1/f$ (1/f noise), then from equation (2.15) the phase noise power $S_{n}(f)$ will vary as $1/f^3$ and will roll off with a slope of $-30$dB/decade. In general, if the noise varies as $1/f^\alpha$, the oscillator's phase noise will vary as $f^{- \alpha - 2}$. It is now clear that the slope of the phase noise as depicted in a semi-log plot of $L(f)$ will indicate the nature of the noise that created it. This is seen on figure 2.6 [9].

By definition, equation (2.9), $L(f)$, is computed as the ratio of the sideband power over the carrier power. While the sideband power is easy to compute in the case of a deterministic noise as previously seen, it is not so easy to compute for an oscillator where the noise is distributed over the spectrum. In equation (2.9), the sideband power is computed over a bandwidth of 1Hz. The total power contained in this 1Hz bandwidth is obtained by integrating the phase noise power over the bandwidth. Because the phase noise power spectrum is often represented on a logarithmic scale it is convenient to have an equation to do the integration in the presence of the logarithmic scale. An equation which allows this is given by Egan [3]:

$$S_{out}(f) = S_{in}(f)|H(f)|^2 \quad (2.16)$$
Here $S_\phi$ is the power spectral density. This integration will give an equivalent modulation signal at the highest frequency of integration. An example of using such a calculation is shown in appendix A.

2.2 Oscillator phase noise model.

2.2.1 Introduction.

In order to minimise the effect of phase noise on a particular system, a good understanding of the mechanisms leading to the up or down conversion of device noise into phase noise is necessary. A quantitative model is hence required for phase noise. Different models have been proposed over the years. The most widely known is the Leeson model [9] which is based on an LC tank oscillator. Unfortunately, it is a semi-empirical model which requires an empirically obtained parameter, called the device excess noise number, to take into account the increase in noise at low frequencies. This limits the usefulness of the model. Other models were proposed but they suffer to a greater or lesser degree from the similar problem of requiring parameters which are not easily obtained from circuits [10], [11]. For these reasons, they are not useful for quantitative results.
Figure 2.6: Typical oscillator phase noise spectrum [9].

More recently Hajimiri [12] proposed a model based on simulation which overcomes the limitation of the previous models. It does not require any fitting parameters, and predictions using the model have proven accurate. It can also be used for various oscillator architectures. Moreover, it gives a clear understanding of how device noise is converted into phase-noise. This insight leads to ways of reducing it. Thus the Hajimiri model gives both qualitative and quantitative results.

Finally, Alper Demir more recently proposed a unified theory of phase noise [2] which, although mathematically rigorous, has the disadvantage of being more complex to apply. The author of this thesis was also content with the reputation of the Hajimiri model at the time of this work.

The next section describes the model proposed by Hajimiri. Further details can be found in [12] and [13]. The method is outlined here and the main equations are introduced.

2.2.2 The Hajimiri model.

The Hajimiri model begins by relating the current noise at a particular node of the oscillator to phase shift; this in effect defines a transfer function. By
combining this transfer function with suitable estimates of the current noise, the phase noise can be predicted.

The transfer function can be obtained by simulation. The simulations involve applying current pulses to the oscillator nodes and measuring the associated phase shift. It is seen that the amplitude of the phase shift depends on the time in the cycle that the current pulse is applied. For instance, applying the current pulse when an oscillator delay unit is saturated low or high will have little effect on the phase. Whereas applying the current pulse at the transition instant of the delay unit will have maximum impact on the phase. This makes the transfer function time varying and periodic. A normalised version of this time varying function is denoted as $\Gamma$. $\Gamma$ is called the Impulse Sensitivity Function (ISF). The phase shift caused by current noise is thus completely described by the ISF; the rms and dc values of this function can be used to compute useful phase noise quantities. Since the method is based on simulation, it is topology independent and does not require any fitting parameters. This function can be found for any type of oscillator. Assuming a ring oscillator made of a chain of delay cells, figure 2.7(a), the current noise at the particular node is computed from the contribution of the devices in the delay element. Combining this current noise with the ISF gives a prediction of the phase noise.

Computing the ISF is summarised in figure 2.7. Figure 2.7(a) shows the waveform of an undisturbed oscillator (solid line). Applying a current pulse at time $\tau$ causes a voltage jump $\Delta V$. This voltage jump results in a phase step $\Delta \phi$ in the waveform (dashed line). The relationship between the current pulse and the phase step can be expressed by a linear periodic time varying transfer function $h_q(t,\tau)$, figure 2.7(c).

The time-varying impulse response of the VCO can be described by:

$$h_q(t,\tau) = \frac{\Gamma(\omega_{osc}\tau)}{q_{max}} u(t-\tau)$$

(2.19)

Where $u(t-\tau)$ is the step function and $\Gamma(\omega_{osc}\tau)$ is the ISF, which is periodic. The term $q_{max}$, which is the maximum charge store on the oscillator node,
normalises the transfer function and allows a degree of freedom in the choice of the amount of charge deposited during the measuring current pulses.

![Diagram of a ring oscillator](image)

Figure 2.7: (a) Ring oscillator, (b) phase shift due to current pulse, (c) impulse response [12].

Since the impulse response $h_0(t,\tau)$ is periodic, it can be expanded as a Fourier series [13] and the excess phase is then given by:

$$\phi(t) = \frac{1}{q_{\text{max}}} \left[ c_0 \int_{-\infty}^{\infty} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{\infty} i(\tau) \cos(n\omega_{\text{osc}} \tau + \theta_n) d\tau \right]$$  \hspace{1cm} (2.20)

Equation (2.20) is the result of a convolution product between the transfer function $h_0(t,\tau)$ and the input current $i(t)$. Equation (2.20) can be used to show how low frequency current noise converts into close-in phase noise and how high frequency current noise is down converted into close-in phase noise. For instance, if $i(t)$ is taken as a low frequency sinusoidal current, that is to say $f_m$ is much smaller than the frequency of oscillation, $f_m << f_{\text{osc}}$ [13]:

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\[ \text{i}(t) = I \cos(\omega_m t) \]  

(2.21)

Then

\[ \phi(t) = \frac{1}{q_{\text{max}}} \left[ c_0 \int_{-\infty}^{\infty} \text{i} \cos(\omega_m \tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{\infty} \text{i} \cos(\omega_m \tau) \cos(n\omega_{\text{osc}} \tau + \theta_n) d\tau \right] \]  

(2.22)

The excess phase \( \phi(t) \) is then composed of the following components:

\[ c_0 \int_{-\infty}^{\infty} \text{i} \cos(\omega_m \tau) d\tau = \frac{c_0 I \sin(\omega_m \tau)}{\omega_m} \]  

(2.23)

\[ \sum_{n=1}^{\infty} c_n \int_{-\infty}^{\infty} \text{i} \cos(\omega_m \tau) \cos(n\omega_{\text{osc}} \tau + \theta_n) d\tau = \]  

\[ = \sum_{n=1}^{\infty} I c_n \left[ \frac{\sin(n\omega_{\text{osc}} - \omega_m) t}{2(n\omega_{\text{osc}} - \omega_m)} + \frac{\sin(n\omega_{\text{osc}} + \omega_m) t}{2(n\omega_{\text{osc}} + \omega_m)} \right] \]  

(2.24)

It should be obvious that because \( f_{\text{osc}} \) is much greater than \( f_m \), the terms weighted by coefficient \( c_1, c_2 \ldots c_n \) and given by equation (2.24) can be neglected. The only term left is therefore the term defined by equation (2.23), thus [13]:

\[ \phi(t) \equiv \frac{c_0 I \sin(\omega_m t)}{q_{\text{max}} \omega_m} \]  

(2.25)

Performing the same analysis for a current noise at a frequency close to the frequency of oscillation \( f_{\text{osc}} \), \( f_{\text{osc}} \pm f_m \) with \( f_m \ll f_{\text{osc}} \), leads to the excess phase composed of the following terms:
\[ c_0 \int_{-\infty}^{\infty} I \cos[(\omega_{osc} + \omega_m)T] d\tau = \frac{c_0 I \sin[(\omega_{osc} + \omega_m)T]}{\omega_{osc} + \omega_m} \]  

Equation (2.26) gives a term that can be neglected due to the presence of \( \omega_0 \) in the denominator. In equation (2.27), the only term of importance is the term obtained for \( n=1 \). All the other terms can be neglected due to the presence of \( n\omega_{osc} \) in the denominator. Therefore, the excess phase in equation (2.20) reduces to [13]:

\[ \phi(t) \equiv \frac{c_1 I \sin(\omega_m t)}{2\omega_{max} \omega_m} \]  

This can be repeated for current noise frequency close to \( 2\omega_{osc}, 3\omega_{osc}, ..., n\omega_{osc} \); in each case, the phase excess can be reduced to [13]:

\[ \phi(t) \equiv \frac{c_n I \sin(\omega_m t)}{2\omega_{max} \omega_m} \]  

The excess phase \( \phi(t) \) described by equations (2.25) and (2.29) modulates the output signal of the oscillator according to equation (2.30):

\[ v(t) = \cos[\omega_{osc} t + \phi(t)] \]  

This corresponds to the simple case of phase modulation studied at the beginning of this chapter. It shows that low frequency current noise is up converted into phase noise around the carrier frequency whereas high frequency current noise is down converted around the carrier frequency.
If phase $\phi(t)$ is small (narrow-band modulation) and we only consider white noise this leads to:

$$L_w(\Delta \omega) = \left( \frac{i^2}{\Delta f \sum_{n=0}^{\infty} c_n^2} \right)$$

(2.31)

Where $i^2/\Delta f$ represents the current noise power density per unit bandwidth. Equation (2.31) is further simplified using Parseval's theorem [6] to:

$$L_w(\Delta \omega) = \frac{i^2}{\Delta f \sum_{n=0}^{\infty} c_n^2}$$

(2.32)

Or, in decibel per Hertz relative to the carrier:

$$P_{\text{disc}} = 10 \log_{10} [L_w(\Delta \omega)]$$

(2.33)

In the 1/f noise region only the dc coefficient, $c_0$, is taken into account [12][13]. Considering that in the 1/f region, the current noise density can be expressed as a function of the white noise power spectrum density and the corner frequency:

$$i^2_{n,f} = i^2_0 \frac{\omega_{1/f}}{\Delta \omega}$$

(2.34)

This leads to the following equation for the 1/f noise part of the spectrum:
An interesting consequence of equation (2.35) is that a small ISF dc value ($c_0$) results in a reduction in the up-conversion of $1/f$ noise into close-in phase noise. Since the dc value of the ISF is directly dependent on fall and rise time symmetry of the oscillator's waveform [13] it is clear that care must be taken in the design of the oscillator to match rise and fall times.

In summary, using equations (2.32) and (2.35), the phase noise spectrum of an arbitrary oscillator is described once the ISF and the node current noise estimates have been obtained from simulations.

Hajimiri has proposed three methods for the computation of the ISF. The first consists of applying a current pulse to each VCO node and recording the corresponding phase shift. This is repeated at regular intervals over one period of the oscillator signal. The current pulse applied must be large enough to cause a measurable phase shift and small enough to comply with a linearity requirement. This requirement constrains the amount of charge dumped onto the node by the current pulse to be a small fraction of the maximum charge stored on the node over a cycle. This is the most accurate method proposed because it involves no simplifications.

A simplification of this method consists of calculating the derivative of the oscillating waveform for each node and then employing equation (2.36) [12], [13] to compute the ISF. This is easily achieved with a little post-processing of the simulation output files. The ISF for a particular node $i$ is obtained using the derivative of the normalised waveform at node $i$ and derivatives of the normalised waveforms at the other nodes:

$$\Gamma(x) = \frac{\sum_{j=1}^{n} f_j^2(x)}{\sum_{j=1}^{n} f_j^2(x)}$$

(2.36)
The number \( n \) of nodes for which the sum in the denominator of equation (2.36) is done can be reduced by making assumptions regarding the contribution of single nodes to the overall phase noise.

A further simplification gives a third method by noting that the summation under the line in equation (2.36) is, in certain cases, approximately equal to the maximum value of the derivative at node \( i \) squared: \((f_{i, \text{max}}'\)^2\). With this, equation (2.36) then reduces to:

\[
\Gamma(x) = \frac{f_i'(x)}{f_{i, \text{max}}'^2(x)}
\]  

(2.37)

This method is the simplest of the three given and is also the least accurate. It is useful for ring oscillators with identical stages [12], [13]. In practice, the oscillator's waveform rarely looks like the one pictured in figure 2.7(b) but looks more like the one described in figure 2.8(a). In this case the ISF can be approximated as two triangles as shown on figure 2.8(b).

Figure 2.8: (a) Oscillator's waveform; (b) corresponding approximate ISF in case of equal fall time and rise time [12].
Depending on the required level of accuracy, one might use any one of the three methods. In the early design iterations the last method can be quite useful because of its simplicity and speed.

2.3. Phase-Locked Loops.

2.3.1 PLL principle.

Among the varieties of frequency synthesizers, the PLL is the most common. Since the PLL has been fully integrated on chip the use of this technique has increased dramatically. Numerous studies on aspects of PLLs have appeared in the literature: [3], [14], [15], [16] and [17]. The frequency multiplication is performed using a negative feedback mechanism to generate an output frequency equal to some number \( N \) times the input frequency. A Phase/Frequency Detector (PFD) is used to provide an error signal which tunes a Voltage-Controlled Oscillator (VCO). Lock is achieved when the output signal's frequency divided by \( N \) is equal to the input signal's frequency and the phases of the two signals are aligned. A block diagram of a PLL is given in figure 2.9.

As long as the system is in lock, the ratio between input and output frequency is \( N \). This means that if the modulus \( N \) of the feedback divider is made programmable, the VCO can be programmed to run at a number of discrete frequencies in a certain range. Along with the VCO, PFD and feedback divider, a filter is used to condition the error produced by the PFD.

2.3.2 Building blocks and their models.

This section reviews some of the most common implementations of the building blocks. Continuous time (Laplace) models for these blocks are also given.
2.3.2.1 Phase/Frequency Detector.

Its purpose is to provide the system with an error signal proportional to the Phase/frequency error between the signals at its two inputs. The simplest PFD is an XOR gate and it can resolve phase errors between ±π. The signals are in lock when their phase difference is π/2. This leads to a strong component at twice the reference clock frequency on the error signal on which the loop can falsely lock [18].

A more complex phase detector commonly used is a sequential PFD which alleviates the false lock problem. This is because its output signals, UP and DOWN are at the same frequency as the input signal. This PFD also has the advantage of being able to resolve phase errors in the ±2π range. Frequency detection mode happens when the phase error is greater than 2π, phase detection mode starts when the frequency has locked and the phase error is less than a cycle [14]. This configuration widens the capture range of the device. It is also used in conjunction with a charge pump. An UP signal when fed into the charge pump has the effect of pumping charge onto the filter and thus increases the voltage on the filter whereas a DOWN signal removes charge from the filter, thereby decreasing the control voltage.
2.3.2.2 Loop filter.

The purpose of the loop filter is to extract the DC component from the output of the PFD. It also fixes the bandwidth of the system and determines its stability. The loop filter can be a passive or active RC filter.

2.3.2.3 Voltage Controlled Oscillator.

The VCO generates the output signal of the synthesiser. The stages in the VCO can be simple inverters or complex differential delay units.

2.3.2.4 Small-signal models.

• Since the average PFD output is directly proportional to the phase error, it can be represented as a simple difference block with a gain $K_{PD}$. This model applies for all PFDs. In the case of a charge-pump PFD, CP-PFD, the gain is equal to the average current flowing into the filter over a cycle:

$$K_{PFD} = \frac{I_{CP}}{2\pi} \quad [A/\text{rad}] \quad (2.38)$$

Where $I_{CP}$ is the charge pump current.

• The Low Pass Filter is represented by a general s-domain impedance term, $LPF(s)$.

• Since the VCO integrates its control voltage with a gain $K_{VCO}$ to produce the VCO's phase, its transfer function in the s-domain is:

$$VCO(s) = \frac{2\pi K_{VCO}}{s} \quad [\text{rad.s}^{-1}/\text{V}] \quad (2.39)$$

• The feedback multiplier is simply represented by a gain
Combining these component models produces a linearised PLL model as follows:

\[
\frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{NK_{vco}K_{\text{LPF}}(s)}{Ns + K_{vco}K_{\text{LPF}}(s)} \quad \text{[rad/rad]} \tag{2.41}
\]

Equation (2.41) applies to almost every PLL; the loop filter used will characterise the difference between PLLs. This formulation can be used during loop design for measuring a number of loop quantities, such as loop bandwidth, acquisition time, input clock suppression and the stability of the loop.

2.3.3 PLL Noise.

Figure 2.10 shows a typical block diagram of a PLL with all possible noise sources in the PLL [19], [20], [21]. If all the noise sources are uncorrelated, superposition applies and this allows the computation of the overall output noise as follows:

\[
\phi_{\text{out}}(s) = \phi_{vco}(s) + \frac{K_{vco}}{s} [N_{\text{LPF}}(s) + \text{LPF}(s)(N_{pbl}(s) + K_{pbl}\phi_e(s))] \tag{2.42}
\]

If the phase error \( \phi_e(s) \) is now defined by:

\[
\phi_e(s) = \phi_{\text{in}}(s) - \frac{\phi_{\text{out}}(s)}{N} - N_{\text{NFB}}(s) \tag{2.43}
\]
Equation (2.42) and equation (2.43) combine to give:

\[ \Phi_{\text{out}}(s) = \Phi_{\text{vco}}(s) + \frac{K_{\text{vco}}}{s} \left[ N_{\text{LPF}}(s) + s \text{LPF}(s) \left( N_{\text{pf}}(s) + K_{\text{pf}} \left( \frac{\Phi_{\text{in}}(s)}{N} - \frac{\Phi_{\text{out}}(s)}{N} - N_{\text{NFB}}(s) \right) \right) \right] \]

Setting all the noise sources to 0 except the input phase noise \( \Phi_{\text{in}}(s) \) and dividing by \( N \) [19], [21], equation (2.44) leads to the transfer function \( H(s) \) defined by equation (2.45):

\[
H(s) = \frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} \bigg|_{N_{\text{PF}}=N_{\text{LPF}}=N_{\text{NFB}}=0} = \frac{K_{\text{pf}} K_{\text{vco}} \text{LPF}(s)}{sN} \frac{1}{1 + \frac{K_{\text{pf}} K_{\text{vco}} \text{LPF}(s)}{sN}}
\]

\( H(s) \) has the following limits:

\[
\lim_{s \to 0} [H(s)] = 1
\]
lim[H(s)]_{s \rightarrow \infty} = 0 \quad (2.47)

This greatly simplifies the noise study. Substituting equation (2.45) into equation (2.44) and rearranging leads to:

\[ \phi_{out}(s) = \phi_{vco}(s)[1 - H(s)] + \frac{N}{K_{lpf} LPF(s)} H(s) \]

\[ + \left[ \phi_{in}(s) - N_{pfb}(s) + \frac{N_{pdf}}{K_{pdf}} \right] NH(s) \quad (2.48) \]

Equation (2.48) represents the total phase noise at the output. Usually the most significant sources of noise are the input noise and the noise generated by the VCO. Also note that each noise contribution except the one made by the VCO is multiplied by N, so in order to limit the noise in the PLL, N should be kept small.

If \( H_{ref}(s) \) is defined as being the transfer function from input noise to output noise, then \( H_{ref}(s) \) is obtained by setting \( N_{lpf}(s) = N_{fbd}(s) = N_{pdf} = \phi_{vco}(s) = 0 \) in equation (2.48). The limits of \( H_{ref}(s) \) for low and high frequency are obtained using the limits of \( H(s) \) when \( s \) tends to zero (equation (2.46)) and infinity (equation (2.47)):

\[ \lim[H_{ref}(s)]_{s \rightarrow 0} = N \lim[H(s)]_{s \rightarrow 0} = N \quad (2.49) \]

The loop is equivalent to a multiplier for the low frequencies.

\[ \lim[H_{ref}(s)]_{s \rightarrow \infty} = 0 \quad (2.50) \]

The loop cancels higher frequency noise. Thus, the loop is a low-pass filter.

Following the same procedure but setting \( N_{lpf}(s) = N_{fb}(s) = N_{pdf} = \phi_{in}(s) = 0 \) this time, the transfer function from the VCO noise, \( H_{vco}(s) \):
\[ H_{vco}(s) = 1 - H(s) \]  

(2.51)

Again, the limits at low and high frequencies of \( H_{vco}(s) \) are obtained using the limits of \( H(s) \). Low frequency disturbances in the VCO are described by:

\[ \lim_{s \to 0} [H_{vco}(s)] = 1 - \lim_{s \to 0} [H(s)] = 0 \]  

(2.52)

Thus the loop tends to reject the slow variations of the VCO. High frequency disturbances in the VCO are described by:

\[ \lim_{s \to \infty} [H_{vco}(s)] = 1 \]  

(2.53)

Thus the loop passes the high frequency variations of the VCO.

To obtain the output power spectrum of the system due to a particular noise source described by its power spectrum, the relationship defined by equation (2.16) is used. Assuming zero correlation between the noise inputs, superposition applies, this is depicted on figure 2.11. Figure 2.11(a) is a plot of the transfer function (in dB) \( H(f) \), the input phase noise characteristic for a crystal (black dashed line) and the resulting output phase noise (solid blue line). Figure 2.11(b) depicts the situation when only the VCO noise source is present, the solid blue line again represents the output phase noise spectrum. Assuming that the two noise sources are independent, superposition applies and the overall response is obtained by adding the response of the PLL to each noise input. This depicted in Figure 2.11(c).
2.4. Delay-Locked Loops.

2.4.1 DLL principle.

The delay-locked loop (DLL) is a circuit that greatly reduces the problems associated with VCO phase noise because there is no VCO. The output signal is delayed by an amount corresponding to the input period such that the two signals are phase aligned. Because the output edge is not re-circulated as in the case of the VCO, phase noise does not accumulate [22], [23]. Instead, the phase error is reset by the next incoming edge of the reference clock. For
correct operation, the delay established by the delay line must be in the range \( T_{\text{ref}}/2 \) and \( 1.5T_{\text{ref}} \)[18]. The building blocks are basically the same as for the PLL with the VCO replaced by a Voltage-Controlled Delay Line (VCDL). The DLL block diagram is shown on figure 2.12.

![Figure 2.12: DLL block diagram.](image)

A DLL can be approximated as a first order system and, close to lock, its transfer function is given by [24]:

\[
\frac{D_{\text{out}}(s)}{D_{\text{in}}(s)} = \frac{1}{1 + \frac{s}{\omega_N}}
\]

(2.54)

Where \( D_{\text{out}} \) and \( D_{\text{in}} \) are output and input delays respectively. This linear model holds for refresh rates of at least ten times larger than the system bandwidth \( \omega_N \), which is defined by:

\[
\omega_N = \frac{f_{\text{ref}} I_{\text{cp}} K_{\text{DL}}}{C}
\]

(2.55)

Where \( f_{\text{ref}} \) is the frequency of the reference, \( I_{\text{cp}} \) the charge pump current (assuming a charge-pump PFD), \( K_{\text{DL}} \) the gain of delay line in \( \text{s/V} \) and \( C \) the value of the capacitor used as filter.
2.4.2 DLL Noise.

The main source of noise will come from the input and from delay elements in the VCDL, this is represented in figure 2.12:

![Diagram of DLL with noise source]

Figure 2.13: DLL with noise source.

Where G(s) is the direct gain of the DLL: \( \omega_N/s \). The transfer function from noise input to output is:

\[
\frac{D_{\text{out}}(s)}{N(s)} = \frac{1}{1 + \frac{\omega_N}{s}}
\]

From which it is clear that for high frequencies, the output noise is equal to the VCDL output noise. Note that for this structure, noise on the input clock, within the bandwidth of the DLL, is transferred directly to the output clock, because each output cycle is started by the input clock.

2.5. Conclusion.

Phase noise has been introduced by examining the spectral power in a simple signal with a deterministic phase modulation of known amplitude and frequency. The results were then generalised to cater for random fluctuations. The relationship between the power spectrum and the phase noise was introduced. Models for phase noise were discussed. Some details of a phase
noise model suitable for design were given. PLLs and DLLs were also introduced with a description of their operation. Finally linear models were described for these devices along with manipulations which show how noise sources in these devices are shaped by the synthesiser systems.

2.6. Reference.


3.0 Introduction.

Delay cell based oscillators can be divided in two types: single-ended and differential. The synthesiser designed in this thesis used a differential VCO structure, but in this chapter two other single ended VCO architectures were investigated to see if they were more suited for the target video application. Typically single-ended structures have better phase noise but they suffer from poor common mode noise rejection. In this chapter some computations are done to investigate these claims. For the analysis the power budget allowed for all of the structures was set at the same level and the VCOs were designed to operate at similar frequencies. The chapter compares the three architectures from a phase noise perspective using the Hajimiri model. This is followed by examining the impact of common mode noise on the device performance. The common mode noise sources analysed are the supply and substrate noise since these are recognised as the most significant for large ASICS [1], [2].

3.1 Ring oscillator phase noise.

3.1.1 Single-ended current starved oscillator (CSO) (Architecture 1).

Single-ended oscillators are the most straightforward in that they use simple CMOS inverters as delay elements. Typically, tuning is achieved by
controlling current supplied to the inverters in figure 3.1 [3]. In this diagram, transistors M4 and M5 form the inverter while M3 and M6 limit the current in the inverter by varying the bias on their gates [4].

The oscillating frequency is influenced by four factors:

- \( N \), the number of stages in the ring.
- \( C_{\text{tot}} \), the total load capacitance between each stage, equation (3.2).
- \( I_{\text{d}} \), the current flowing in the delay stage.
- \( V_{\text{DD}} \), the supply voltage.

The frequency of oscillation is given by equation (3.1):

\[
f_{\text{osc}} = \frac{I_{\text{d}}}{N C_{\text{tot}} V_{\text{DD}}} \quad \text{[Hz]} \quad (3.1)
\]

The total capacitance on any node of the oscillator is given as [3]:

\[
C_{\text{tot}} = \frac{5}{2} C_{\text{oX}} \left( W_4 L_{\text{eff}4} + W_5 L_{\text{eff}5} \right) \quad \text{[F]} \quad (3.2)
\]

\[
L_{\text{eff}4} = L_{\text{eff}5} = L - 2L_d \quad \text{[m]}
\]

\[
L_d: \text{lateral diffusion}
\]

\[
C_{\text{oX}} = \frac{3.97 \epsilon_0}{t_{\text{oX}}} \quad \text{[F/m}^2\text{]} 
\]

For the TSMC 0.25\( \mu \text{m} \) process the lateral diffusion is \( L_d = 0.12 \mu \text{m} \) and the oxide thickness \( t_{\text{oX}} = 5.4 \text{nm} \).

In order to study the phase noise of such a structure, an eleven stages CSO has been designed for an output frequency of 111MHz with a power consumption of 1.5mW. The oscillator’s delay stage is designed for equal rise time and fall times. This is achieved by equalising the drive strength of transistor M4 and M5. Assuming the same threshold voltage for P and N channel MOS devices and that the mobility of the electron, \( \mu_{\text{N}} \), is roughly three times larger than the mobility of the holes, \( \mu_{\text{P}} \), this implies that the width of M4 must be three times that of M5.
Oscillator output

Figure 3.1: Five stages Current Starved ring Oscillator (CSO).

The width and lengths of all transistors are as follows:

<table>
<thead>
<tr>
<th>Transistor</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L</td>
<td>18/0.75</td>
<td>9/0.75</td>
<td>18/0.75</td>
<td>9/0.75</td>
<td>3/0.75</td>
<td>6/0.75</td>
</tr>
</tbody>
</table>

Table 3.1: Device sizes for the Current-Starved Oscillator.

Using these parameters the total capacitance $C_{tot}$ is found to be equal to 99.55fF. With this, the maximum charge $q_{max}$ is computed to be 248.9fC (2.5 volts voltage swing).

The phase noise is obtained using Hajimiri’s model (chapter 2). Three nodes per stage influence the output phase noise: the node that connects two stages, the drain of M6 and the drain of M3 (figure 3.2(a)). An ISF (see chapter 2) for each node was computed by applying a current impulse at each point in the oscillation cycle. This is shown in figure 3.2(a).
The charge deposited was kept small enough to comply with the Hajimiri linearity requirement but big enough to allow accurate measurements of phase shift. The phase shift is measured a few cycles later. The ISFs obtained using the direct method for each of these nodes are shown in figure 3.3.

The shape of the ISFs from nodes marked PMOS and NMOS in figure 3.3 is explained by the fact that only the two PMOS transistors are connected to the...
output node during the rise time (figure 3.2(b)) while only the two NMOS are connected to the output node during the fall time (figure 3.2(c)).

Because of the equal fall time and rise time, the dc value of the ISF of the node MID is close to zero. From this only the white noise from the two transistors connected to the inverter node MID contribute to phase noise. This is not the case for the NMOS and PMOS transistors forming the current sources. Their ISFs have large dc values and it is expected that their 1/f noise will dominate the phase noise spectrum at low frequency. The dc and rms values for the three ISFs are summarised in table 3.2.

<table>
<thead>
<tr>
<th>ISF</th>
<th>$\Gamma_{dc}$</th>
<th>$\Gamma_{rms}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>MID</td>
<td>0.01489</td>
<td>0.199494</td>
</tr>
<tr>
<td>PMOS</td>
<td>0.234389</td>
<td>0.104844</td>
</tr>
<tr>
<td>NMOS</td>
<td>-0.218845</td>
<td>0.0643697</td>
</tr>
</tbody>
</table>

Table 3.2: ISF parameters for CSO.

The biasing circuit noise contribution must be taken into account. In [5], the biasing circuit contribution for a differential ring oscillator is investigated. This study shows that the contribution of the biasing circuit can be reduced by using small multiplication factors in the current mirror. This is explained by the fact that the noise from the biasing transistor $M_{bias}$, figure 3.4, is mirrored to each delay element with gain $m$, therefore the noise power is amplified with gain $m^2$:

$$\left(\frac{\overline{i_i^2}}{\Delta f}\right)_{M_{1\ldots M_n}} = m^2 \left(\frac{\overline{i_i^2}}{\Delta f}\right)_{M_{bias}} \quad [\text{A}^2/\text{Hz}] \quad (3.3)$$
The drain current noise (white) of a MOS transistor is given by [6], [7], [8]:

\[
\frac{i_n^2}{\Delta f} = 4kTg_{d0}
\]  \hspace{1cm} [\text{A}^2/\text{Hz}] \hspace{1cm} (3.4)

Where \( T \) is the temperature in Kelvin and \( k \) is Boltzmann's constant, \( g_{d0} \) is a parameter which has a value of 2.5 for short channel devices [9]. Finally \( g_{d0} \) is the channel conductance at zero bias. The current noise of transistor \( M_{\text{bias}} \) is equivalent to having an additional source of noise on each PMOS current source with current noise power:

\[
\frac{i_n^2}{\Delta f}_{\text{add}} = \frac{4kTymg_{d0}}{N}
\]  \hspace{1cm} [\text{A}^2/\text{Hz}] \hspace{1cm} (3.5)

Where \( g_{d0} \) is the zero-bias conductance of the PMOS current source and \( N \) is the number of stages in the oscillator. This can be verified by first introducing a sinusoidal disturbance \( I_n \) in parallel with \( M_{\text{bias}} \) (figure 3.4) and computing the FFT of the output signal of the VCO to obtain the power spectrum. The result of such an FFT is shown as the solid line in figure 3.5. The sinusoidal current has an amplitude of 10\( \mu \)A and a frequency of 15MHz. It is injected in parallel with \( M_{\text{bias}} \), figure 3.4. Secondly, injecting a sinusoidal current of amplitude 10/\( \sqrt{N} \) \( \mu \)A (with \( N=11 \)) at a frequency 15MHz in parallel with each PMOS tail transistor (\( M_1, M_2 \ldots M_N \)) should have the same effect. An FFT is run on the
output signal of the oscillator and the result is shown in figure 3.5 as the red curve.
Both spectra have two significant peaks at an offset of 15MHz away from the carrier. In both cases the relative peak power to the carrier is -25dBC. These peaks also show that low frequency noise from the current sources and from the bias are strongly up-converted into close-in phase noise.

\[ N = \frac{4kT \gamma_{d0,p}}{m} + \frac{4kT \gamma_{E_{d0,p}}}{N} \]  (3.6)

From equation (3.6) the current mirror gain \( m \) must therefore be kept low to reduce the effect of the biasing circuit. In the CSO studied here, \( m \) is set to 1.

The noise defined by equation (3.6) is combined with the ISF of node PMOS...
(figure 3.2) to produce the phase noise contribution from the PMOS current source (figure 3.5).

The current noise contribution of the inverter M4 and M5 is given by [11]:

\[
\left(\frac{i_n^2}{\Delta f}\right)_{av} = 8kT \gamma_{g_{ds}} [\text{Hz}] \quad (3.7)
\]

The noise defined by equation (3.7) is combined with the ISF of node MID (figure 3.2) to produce the phase noise contribution from the inverter transistors (figure 3.5).

The current noise contribution of the NMOS current source is:

\[
\left(\frac{i_n^2}{\Delta f}\right)_{N} = 4kT \gamma_{g_{ds},N} [\text{Hz}] \quad (3.8)
\]

This noise is combined with the ISF of node NMOS (figure 3.2) to produce the phase noise contribution from the NMOS current source (figure 3.5).

Combining all these contributions gives the overall phase noise spectrum \(S_p(f)\). The noise spectrum for each node as well as the overall spectrum is shown in figure 3.4.
Figure 3.6 clearly shows that the lower part of the phase noise spectrum is dominated by the 1/f noise of the NMOS and PMOS transistors forming the current sources while the higher frequency phase noise is dominated by the white noise due to the inverters. As a reference point we note that at an offset of 1MHz the phase noise is $-121\text{dBc/Hz}$.

For completeness the phase noise is recomputed using the steady-state solution of the waveform. This method (first derivative method) which was described in chapter 2 uses equation (2.37). The following figure compares the ISF for node MID using the direct method and the first derivative method (equation (2.37)).
Figure 3.7: ISF for node MID using the direct method (blue curve) and the first derivative method (red curve).

A further comparison of the two methods is given in table 3.3 where, the dc and rms values of the ISFs are reported for each method.

<table>
<thead>
<tr>
<th>ISF MID</th>
<th>$\Gamma_{dc}$</th>
<th>$\Gamma_{rms}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct method</td>
<td>0.01489</td>
<td>0.199494</td>
</tr>
<tr>
<td>First derivative method</td>
<td>0.000878</td>
<td>0.1917</td>
</tr>
</tbody>
</table>

Table 3.3: ISF parameters for CSO using direct and first derivative methods.

The rms values are very similar while the dc values differ significantly. As a final comparison the phase noise spectra (white) computations for the two methods are plotted in figure 3.6. For this architecture they give similar results.
3.1.2 Single ended with variable capacitors (Architecture 2).

It is also possible to obtain a variable delay using simple CMOS inverters and voltage controlled capacitors [4], [10]. A topology using this idea is shown in figure 3.9. The sizing of the MOS devices is again calculated to produce equal
drive for the NMOS and the PMOS. This in turn produces equal rise and fall time [11].

This oscillator has again been designed for an output frequency of 111MHz when the control voltage is 1.25 Volts (VDD/2). The oscillator consumes roughly the same power as the previous architecture (1.13mW). The load capacitor is the sum of the input and output capacitance of the inverters. Equation (3.2) is used with the appropriate values and an addition is made for the two tuneable capacitors. The tuneable capacitors are realised using the distributed structure of a MOS transistor, figure 3.10(a) [8]:

As the gate voltage increases, the distributed resistors decrease and the node sees more capacitance thereby increasing the delay. Note that one side of the capacitor is floating (figure 3.9), thus the drain current $I_{DS}$ is null. This was simulated by connecting the drain (source) of the PMOS (NMOS) capacitor to VDD (GND) through a large (10GΩ) ideal resistor as shown in figure 3.10(b). Because there is no DC current flowing, these capacitors do not add 1/f noise. In [8], the local white fluctuations $S_{in}$ in parallel with each resistor in figure 3.10 is proportional to $I_{DS}$. Thus their contributions can be neglected. The total node
charge was calculated from simulation to be 370fC. The inverter contributed 248.8fC to this number (equation (3.2)).

All nodes in the oscillator are identical, therefore a single ISF characterised the structure. Again, two different methods were used to calculate the ISF: the direct method and the first derivative method. The results are shown in figure 3.11. Note that the symmetry criterion (low DC components) is well respected. Table 3.4 compares the dc and rms values obtained with both methods.

<table>
<thead>
<tr>
<th>ISF</th>
<th>$\Gamma_{dc}$</th>
<th>$\Gamma_{rms}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct method</td>
<td>0.0113649</td>
<td>0.117206</td>
</tr>
<tr>
<td>First derivative method</td>
<td>0.0091166</td>
<td>0.127525</td>
</tr>
</tbody>
</table>

Table 3.4: ISF parameters using two different methods.

Again at a reference point of 1MHz from the carrier the phase noise is -130.6dBc/Hz. This shows an improvement of 9dB over the CSO. It can be seen that the current sources in a single-ended current-starved VCO introduce a significant amount of noise (mainly in the $f^3$ region) even if the delay stages are designed for equal rise and fall times.
3.1.3 Differential delay unit (Architecture 3).

A widely used topology for ring oscillators is the differential ring oscillator. The delay elements are differential gain stages. This allows the oscillator to reject common mode noise such as substrate and supply noise. These noise sources are usually dominant if the oscillator is implemented in a VLSI application where the switching of digital circuits cause supply variation and substrate noise [12], [13], [14].

The delay element is shown in figure 3.13. The delay is based on an RC time constant and is made variable by varying the value of the load resistor. The Voltage-Controlled Resistor (VCR) is a simple connection of MOSFETs [12]. The capacitance represents the load capacitance of the next stage and the output of the driving stage.

Figure 3.12: Simulated phase noise spectrum for simple oscillator using the direct method.
The delay stages were designed to provide equal rise time and fall time in order to reduce low-frequency noise up-conversion into close-in phase noise [11]. Under this condition, $\bar{i}^2/\Delta f$ is only due to the white noise contributions of the differential pair and the load. The noise generated in the tail can also be neglected [11]. Although the current noise density $\bar{i}^2/\Delta f$ is bias dependent, it was shown in [11], [15] that its evaluation at mid-transition is a valid approximation in the case of a ring oscillator, and thus, $\bar{i}^2/\Delta f$ in equation (2.32) is given by [11] [15]:

$$
\frac{\bar{i}_m^2}{\Delta f} = 4kT I_{\text{tail}} \left( \frac{\gamma}{E_C L_{\text{diff}}} + \frac{1}{R_{\text{VCR}} I_{\text{tail}}} \right)
$$

[A^2/Hz] (3.9)

Where $I_{\text{tail}}$ is the tail current. $T$ is the temperature in Kelvin and $k$ is Boltzmann's constant. $E_C$ is the critical electrical field and has a value of $4 \times 10^6$ V/m (typical value for sub micron process) [16]. This actual value used was extracted from the device's model and is valid for NMOS and PMOS. $R_{\text{VCR}}$ is the effective resistance value of the VCR. Finally $\gamma$ is a parameter which has a value of 2.5 for short channel devices [9]. The first term in brackets corresponds to the
differential pair noise contribution and the second term is the VCR’s contribution.

Using the same model as before the phase noise spectrum was calculated and it is shown in figure 3.14.

![Phase noise spectrum](image)

**Figure 3.14: Simulated phase noise spectrum for differential VCO using the direct method.**

At an offset of 1MHz the phase noise is white and has a value of -108.5 dBc/Hz. This figure is significantly worse than the two single ended oscillators and this is explained by the following two factors:

- increased complexity in obtaining perfect symmetry in the waveform.
- increase in the number of noise sources.

Of these two factors, the increase in the number of noise sources is the more significant.

### 3.2 Phase noise comparison of the three architectures.

In the following table the phase noise at an offset of 1MHz for the three oscillators are given:
### Table 3.5: Phase noise comparison.

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>Phase noise at 1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSO</td>
<td>-121.1dBC/Hz</td>
</tr>
<tr>
<td>Variable capacitor</td>
<td>-130.56dBC/Hz</td>
</tr>
<tr>
<td>Differential</td>
<td>-108.5dBC/Hz</td>
</tr>
</tbody>
</table>

The simulated phase noise spectrum for the three oscillators is shown in figure 3.15.

From the above table and figure it is obvious that the single-ended oscillator with variable capacitors outperforms the two other topologies. This is due to the small number of noise sources (only two MOS devices forming the inverter) and the fact that balancing the drive strength of these devices is easy.

Unfortunately, this is only a part of the picture. The Hajimiri model does not cater for sources of noise external to the delay element. These include supply and substrate noise. Typically these noise sources are caused by switching in digital sections on a chip and as a result they are deterministic. If these deterministic components of noise are large this may offset any improvements.
in phase noise seen in the single ended architecture. Studies have shown that these components are significant [2]. The next sections will attempt to quantify the effects of these noise sources.

### 3.3 Supply and substrate noise.

VDD noise can be evaluated by simulating the circuits with a small amplitude sinusoidal addition to VDD. Substrate noise is modelled as a sinusoidal upset to the bulk of some of the devices in the VCO. For the three architectures studied in the previous sections, a 10mV [17] sinusoid with a frequency of 15MHz is applied to VDD and to all the bulks of the NMOS devices in the inverters. The next section shows the resulting effects on the oscillator frequencies. To help quantify the results, an FFT of the VCO's output was computed.

#### 3.3.1 CSO (Architecture 1).

Figure 3.16 shows the results of VDD noise on the output spectrum for the CSO. The sinusoid gives rise to two significant peaks around the carrier (-25dBc/Hz). The result for a 10mV sinusoid on the bulk of the NMOS in the inverter is shown in figure 3.17:

Converting this value to equivalent jitter by noting that for a single ray (figure 2.3):

$$10 \cdot \log_{10} \left( \frac{m^2}{4} \right) = -25 \text{dBc/Hz}$$

The total power for the two rays is -25dB + 3dB = -22dB, so:
\[
\frac{m}{\sqrt{2}} = \sqrt{10^{-22}} \quad \text{[rad rms]} \quad (3.11)
\]

Dividing equation (3.11) by the frequency of oscillation \( \omega_0 = 2\pi f_0 \) gives the rms timing jitter [18]:

\[
\tau_j = \sqrt{\frac{10^{-22}}{2\pi f_0}} \quad \text{[s rms]} \quad (3.12)
\]

For this study \( f_0 \) is set at 111MHz, so \( \tau_j = 114 \text{ps} \).

This simple simulation shows that current starved inverter based ring oscillators are very sensitive to common mode noises that are typically found in ASICs.

Figure 3.16: CSO output voltage waveform spectrum with a 10mV sinusoid at frequency 15MHz on VDD.
3.3.2 Simple oscillator (Architecture 2).

The same simulations are carried out for the simple inverter oscillator. Figure 3.18 shows the results of VDD noise on the output spectrum. The sinusoid gives rise to two significant peaks around the carrier (-35dBc/Hz).

The result for a 10mV sinusoid on the bulk of the NMOS in the inverter is shown in figure 3.19. The absence of any significant peaks show that this noise has minimal effect on the spectrum.

The sidebands due to the sinusoidal noise on VDD gives an rms timing jitter of:

\[ \tau_j = \sqrt{\frac{-35 \times 10^{-10}}{2\pi f_0}} \]  

[rad rms] (3.13)

And with \( f_0 = 111 \text{MHz} \), \( \tau_j = 36 \text{ps} \).
Figure 3.18: Simple oscillator’s output voltage waveform spectrum with a 10mV sinusoid at frequency 15MHz on VDD.

Figure 3.19: Simple oscillator’s output voltage waveform spectrum with a 10mV sinusoid at frequency 15MHz on the NMOS inverter’s bulk.

3.1.3 Differential oscillator (Architecture 3).

The experiment is repeated for the differential oscillator with the same level of noise applied. Figure 3.20 shows the resulting output spectrum if VDD is
disturbed by a 15MHz sinusoid with a 10mV amplitude. As can be seen there are no significant peaks around the carrier at an offset of 15MHz, as expected. Figure 3.21 shows the resulting output spectrum if the bulk of the PMOS differential pair is disturbed by a 15MHz sinusoid with a 10mV amplitude. Again, there are no significant peaks around the carrier at an offset of 15MHz, as expected.

The sidebands due to the sinusoidal noise on VDD or on the PMOS bulk gives an rms timing jitter of:

$$\tau_j = \frac{\sqrt{10^{-55/3}}}{2\pi f_0} \text{ [rad rms]} \quad (3.14)$$

And with $f_0 = 98$MHz, $\tau_j = 4.07$ps which is a significant improvement by factors of 28 and 10 compared to the results obtained for the CSO and the simple oscillator respectively.
3.4 Conclusion.

In this chapter, three oscillators with different structures have been studied. The Hajimiri model was used for each of them to obtain quantitative random phase noise figures. In addition, the effects of deterministic VDD and substrate noise sources were investigated. To summarise the study, a listing of advantages and drawbacks of each oscillator is given in table 3.6.

<table>
<thead>
<tr>
<th>Number of MOS per stage</th>
<th>Dependence of phase noise on number of stage [15]</th>
<th>1/f noise up-conversion</th>
<th>Sensitivity to common mode noise</th>
<th>Ease of meeting Hajimiri criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSO</td>
<td>4</td>
<td>No</td>
<td>high</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>easy</td>
</tr>
<tr>
<td>Single ended</td>
<td>4</td>
<td>No</td>
<td>low</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>easy</td>
</tr>
<tr>
<td>Differential</td>
<td>12</td>
<td>Yes</td>
<td>high</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>hard</td>
</tr>
</tbody>
</table>

Table 3.6: Oscillators summary.
It is clear that the choice of architecture for an oscillator is a compromise between phase noise and robustness in the presence of noise. For a noise free environment, a single-ended structure might be used. For noisy VLSI applications a differential structure should be used because of its ability to reject supply and substrate disturbances.

Typical applications for which the frequency synthesiser discussed in this thesis will involve a large mixed-signal IC. Another feature of the target application is that it allows many cycles of the VCO run open loop without correction from the input clock. The digital circuitry on the IC will generate a significant amount of noise in the supply, ground and substrate. This noise can produce significant jitter in single ended structures and furthermore these effects might accumulate over the many open loop cycles of the VCO. This suggests that the differential structure is more suitable for the target video application than single ended structures. Carefully designing the delay cells using the Hajimiri model and optimising the bias circuitry surrounding the chain of delay elements should reduce the impact of a naturally higher phase noise device for the differential delay cells.

3.5 Reference.


Chapter 4
Factorial DLL:
design and analysis

4.0 Introduction.

Typical video synthesisers accept input clock frequencies in the tens of kHz and produce output frequencies in the tens of MHz. The challenge with these synthesisers is concerned with the fact that the input clock frequency is low with respect to the $1/f$ noise components in CMOS oscillator structures which are normally used for clock generation. This noise causes the output clock to drift between phase updates of the input clock. For video applications this phase drift is a key performance parameter. When the phase drift is significant, pixels are lost from a video screen.

One way to tackle this clock multiplication problem is to use a standard Phase-Locked Loop (PLL). In the PLL the input clock is used to phase adjust the clock of a CMOS oscillator. When the adjustment of the phase is slow with respect to noise signals in the oscillator, the oscillator output drifts significantly between cycles of the input clock. Furthermore, in the PLL, a phase error produced during one input cycle is re-circulated because in a ring oscillator the end of a particular cycle starts a new cycle. This re-circulation leads to an accumulation of phase drift, which exacerbates the problem.

A Delay-Locked Loop (DLL) is another circuit topology used for clock multiplication. It minimises the phase drift accumulation problem. In this architecture the reference clock provides an input for a Voltage-Controlled Delay Line (VCDL). When in lock, the VCDL delays the signal by exactly one period of the input signal such that input and output edges are aligned. To generate the higher frequency clock a number of evenly spaced taps are taken
from the VCDL and logically combined. Because each cycle of the output clock is started by the incoming clock there is no recycling of phase error within the delay line. The problem with the DLL structure however is that it can not be used for large output to input clock ratios. The reason for this is that it would require a very large logic depth to combine the delayed signals for the production of the output clock and this results in skew problems which degrade the resulting clock. Furthermore the structure would contain too many delay stages to be practical.

A hybrid circuit is the factorial DLL [1], [2]. In this topology a ring oscillator is formed for the duration of the reference clock period. This feature allows high clock multiplication ratio. The arrival of a new input clock edge restarts the VCO and resets the phase error to zero. In [1], the circuit was designed to show that it was possible to design a clock synthesiser using only CMOS standard cells. This meant that the device was purely digital. A variable delay is achieved by selecting an output signal from various points along a chain of fixed propagation delay logic inverters. Oscillations are generated by continuously setting and resetting a flip-flop. The multiplication range is limited to 20 in the reported device. In [2] higher multiplication ratios were introduced but the delay elements and architecture used were not optimised for low noise and the results show significant drift. This second circuit does not use fixed-delay inverters in the delay chain but current starved inverters which allow a higher delay range. These inverters suffer from poor common mode noise rejection as seen in chapter 3. As a result the substrate and supply noise significantly degrade the performance of this device. This synthesiser was shown to be capable of frequency multiplication ratios of up to 2000 however. The main difference between the circuits in [1] and [2] is the way the delay elements are implemented. A significant feature of both circuits is that they are periodically resynchronised and this avoids phase error accumulation.

The approach taken in this thesis is to configure the chain of delay elements as a ring oscillator and periodically configure it as a delay line rather than setting and resetting a flip-flop. In order to reduce phase drift, the delay elements are optimized for low phase noise using the Hajimiri criteria of equal
rise time and fall time. A differential architecture was chosen to reject common mode noise such as supply and substrate noise.

This chapter is organised as follows. The two previous FDLLs are briefly explained. The principle of action of the synthesiser designed in this thesis is then explained. The architecture of the delay line is discussed and the sources of noise in the circuit are identified. The theoretical phase noise spectra for two possible delay chains are obtained using the Hajimiri model. The effect of the control loop on these noise spectra is then investigated. Finally, some of the other building blocks are explained.

4.1 System description.

The Factorial (or Factorised) Delay-Locked Loop circuit is basically a DLL structure in which the chain of delay elements is configured as an oscillator is then periodically switched into a delay line. The circuit presented in [1] shown in Figure 4.1 is based on a set-reset flip-flop and two variable delay elements. The delay elements are made of a series of fixed delay inverters. The delay control is accomplished by multiplexing a number of different points along the array of inverters. The flip-flop is clocked by the reference clock (CKREF). A rising edge on CKREF causes the flip-flop output to go high. This edge is then delayed by the first delay element with delay $6t$. This edge is then used to reset the flip-flop. The output of the first delay element is also fed to a second delay element of equal delay, $\delta t$. The output of this second delay element is used to set the flip-flop after a delay $2\delta t$. This edge is also used for phase comparison with the input. These happen N times (N is set by a counter) after which, the feedback divider allows a new edge on CKREF to start the cycle again. The value of the delay $\delta t$ is digitally adjusted (multiplexor control) to find the lock position. The maximum multiplication factor for this particular circuit is 20. The circuit presented in [2] is based on the same architecture but it implements the variable delay differently. It achieves multiplication factors of up to 2000
from input clock frequencies ranging from 32kHz to 150kHz. The delay element used here is a series connection of current starved inverters. This type of inverter suffers from poor supply noise rejection but it is a straightforward configuration.

![Diagram of Factorised Delay-Locked Loop](image)

Figure 4.1: Factorised Delay-Locked Loop [1].

The circuit designed for this thesis does not use a set-reset flip-flop to generate the multiplied clock. Instead, the output signal of the chain of delay elements is directly fed back to its input to form a voltage-controlled oscillator. To allow for oscillation conditions either an odd number of cells is used or an extra signal inversion is added in the chain. This structure is shown in figure 4.2(a). The structure has two switches at its input to select which of the two signals, reference clock or output clock, is to be fed to the device. The two switches are controlled by a signal, S1, which is generated using a counter. This sets the multiplication ratio between input and output clocks.

For example a 3X clock is produced by closing S1 (S2 open) and allowing the rising edge of the input clock into the delay line. S1 is then opened and S2 is closed to allow the input clock re-circulate for three cycles. After three cycles S2 is reopened and the process repeats.

Assuming $t_d$ is the delay established by a single delay cell, $N$ is the number of delay cells and $M$ the multiplication factor, the overall delay is:
$$T_{\text{delay}} = 2Nt_dM \quad (4.1)$$

Where $2Nt_d$ is the delay needed to accomplish one cycle of the output frequency (Phi5). In the structure, the reference edge has to pass $M$ times through the device.

The operation of the device is completed with a phase comparison between the third edge of the re-circulating signal and the next incoming edge. An error between these edges is used to adjust the delay through the loop until the incoming clock edge is in phase with the re-circulated edge.

A complexity of the scheme is that the switching of the clock source from input clock to fed-back clock needs an early warning signal. To provide this an early phase (Phi2 in figure 4.2) is used. This signal is used to select the edge for the VCDL line and activate the phase frequency detector which measures the phase error between incoming and fed-back clock edge. Figure 4.3 shows the complete system with a programmable counter which determines the input to output clock multiplication, a filter to condition the error signal and a clock enable block to allow appropriate phase frequency detection. Figure 4.3 also shows a standard PLL which does a final clock multiplication on the output of the block. This is a standard PLL which will have a high input refresh rate ($F_{\text{clock}}$) and thus it adds no phase drift. This PLL allows for greater flexibility in selecting the multiplication ratio.
Figure 4.2: VCO/VCDL principle (a) device, (b) waveform for x3.

Figure 4.3: Complete block diagram.
To get a better understanding of how the device attains lock, the situations where the output clock is too fast and when it is too slow are now explained in detail.

If the output clock leads the reference clock, the system needs to be slowed down and the corresponding waveforms are shown in figure 4.4. In this case, the VCO switches from VCO mode to VCDL mode and waits for a falling reference edge to restart the sequence. Once the edge has reached Phi2 it toggles the device back to VCO mode.

Figure 4.4: Waveforms when output clock leads the reference clock: System is slowed down.
Conversely, if the output lags the reference clock, the system needs to be sped up. The corresponding waveforms are shown on figure 4.5. In this case, the window signal has a smaller duration and the last period of VCO oscillation is truncated.

Figure 4.5: Waveform when output clock lags the reference clock; System is sped-up.

Unlike the FDLL in [1] where the delay is initially set to a suitable value, the FDLL presented here gradually builds up the control voltage to a value allowing the chain of delay elements to process the signal.
4.2 Design for low noise.

4.2.1 Delay element and delay line.

If a jitter free clock source is used to drive this device, most of the noise will be generated in the VCDL. With this in mind, the noise in the delay chain must be minimised to optimise the performance of the device. First of all, a choice between single ended or differential architectures must be made. A single ended design will have less intrinsic noise sources but chapter 3 showed that single ended architectures have significant sensitivity to common mode noise. Because of this, the single-ended architecture is not suitable for integration. Interlacing two single-ended ring oscillators can alleviate this problem somewhat [4], but again this approach may not be adequate in a noisy system chip. A more robust delay line architecture uses the differential delay element. This has more intrinsic noise but it rejects common mode noise (chapter 3). The differential delay unit is seen in figure 4.6. It uses a PMOS source-coupled pair along with a linear voltage-controlled resistor load (VCR). When designing with this structure, load linearity is essential to minimise supply noise impact on timing jitter [5] and to improve low-frequency noise up-conversion into phase noise [6]. Note that the well of the source-coupled pair is not connected to VDD but is tied to a quiet voltage reference. This has the effect of suppressing noise injected from the supply [7].

Twenty such differential delay cells are used to form the delay line. Groups of four form one single delay element as shown on figure 4.7. Crossing connections between two source-coupled pairs provides the necessary phase-inversion to guarantee oscillation once the chain of twenty delay elements is configured as a ring, figure 4.7.

The delay stages were designed to provide equal rise time and fall times in order to reduce low-frequency noise up-conversion into close-in phase noise. Under this condition, $\frac{\gamma}{\Delta f}$ is only due the white noise contributions of the differential pair and the load, equation (3.3). The noise generated in the tail can be neglected as explained in [6]. Equation (3.3) is repeated here for convenience:
\[
\Delta f = 4kT I_{\text{tail}} \left( \frac{\gamma}{E_C L_{\text{diff}}} + \frac{1}{R_{\text{VCR}} I_{\text{tail}}} \right) \quad [\text{A}^2/\text{Hz}]
\] (4.2)

Because phase \( \Phi_2 \) is used to control the input switches, it needs to be converted to a single ended signal. \( \Phi_5 \) is also level shifted and converted to a single ended signal as it drives the edge selector which is implemented using digital gates. Figure 4.8 shows the complete delay line, including the level-shifters:
4.2.2 Replica biasing.

The level of the voltage swing in the delay element must also be reasonably fixed to ensure stable operation over process variations and temperature. If the swing is maintained, the tail current to the stage can be used to set the resistance of the VCR. The voltage swing across the VCRs is fixed by means of a replica biasing circuit along with a bandgap reference circuit, figure 4.9 [7]. The feedback loop adjusts the output of the amplifier such that the voltage drop across the VCR in the replica of the delay cell is equal to the reference voltage when the current from M1 flows. All the VCRs in the delay chain share the same control voltage as the VCR in the replica, that is the output voltage of the operational transconductance amplifier (OTA). As a result they will have the same resistance value as the VCR in the replica. In addition, because the drain current of M1 is mirrored to the delay cells, the same current will flow in all VCRs. Therefore, the voltage across the VCRs in the delay cell is equal to the voltage set across the VCR in the replica and this will be independent of the current in M1. Thus the current can be adjusted to change the resistance and thus change the delay without changing the voltage swing in the delay elements.

This scheme has the advantage of providing a very fixed swing voltage, but the use of an amplifier in the control path has the drawback of introducing a significant 1/f noise component directly onto a sensitive control node in the delay line. This noise causes slow variations of the effective resistance value of
the VCR and the result of this is a slow variation in the delay established in the delay line. The net result is a modulation of the output frequency. This can be represented by a simple gain, $K_{\text{OTAVCDL}}$ (Hz/V) and, for the designed delay line, simulations measured it at 66MHz/V. If $V_n(t)$ is the noise component on the control voltage with spectral density $S_n(f)$, then the frequency fluctuation is simply:

$$\Delta f(t) = K_{\text{OTAVCDL}} V_n(t) \quad \text{[Hz]} \quad (4.3)$$

The phase noise spectral density is then (chapter 2, equation (2.16)):

$$S_{\phi}(f) = \left( \frac{K_{\text{OTAVCDL}}}{f} \right)^2 S_n(f) \quad \text{[rad}^2/\text{Hz]} \quad (4.4)$$

Using equation (4.4) with the simulated output noise spectral density of the OTA, the phase noise spectrum of the VCO is obtained, figure 4.10.
The noise shown in Figure 4.10 between 1kHz and 1MHz has a slope of \(-30\text{dB/decade}\) and thus corresponds to \(1/f\) noise (chapter 2). This shows that the \(1/f\) noise of the OTA produces low frequency variations of the phase over a wide bandwidth. This demonstrates the unsuitability of the replica-biasing scheme as a voltage-swing regulation scheme for low refresh rate applications.

### 4.2.3 Open loop control.

In order to avoid the low frequency noise due to the replica biasing, another scheme is used, figure 4.11. A voltage controlled current source is used to bias the delay element. The area of transistor M2 is made large to significantly reduce the \(1/f\) noise generated by this transistor [8]. With this scheme, there is no major source of \(1/f\) noise modulating the value of the VCR. If the Hajimiri criteria is also satisfied (equal rise and fall times), it is possible to cancel the effect of the \(1/f\) noise present in the tail current of the delay stage. Thus the contribution of the bias circuit to the phase noise spectrum can be neglected. The current \(I\) (figure 4.11) is tuned using the same VCR as in the delay element and, because the source of M2 is effectively pinned by the large \(g_m\) of M2 the current, \(I\) is given by:
\[ I = \frac{V_{\text{ref}} - V_{\text{THN}}}{R_{\text{VCR}}} \]  

Where \( V_{\text{THN}} \) is the threshold voltage of M2 and \( R_{\text{VCR}} \) is the value of the VCR for a given control voltage [3].

\[ R_{\text{VCR}} = \frac{1}{\beta(V_{\text{out}} - V_{\text{THN}})} \]

The current \( I \) is mirrored to the delay element with a gain of \( m \). Assuming M4 fully ON and M5 OFF (and vice versa), M4 has a drain current of:

\[ I_{D}^{M4} = mI \]

The voltage swing is then:

\[ V_{SW} = I_{D}^{M4} R_{\text{VCR}} \]

\[ = mIR_{\text{VCR}} \]

If the control voltage increases, the value of the VCR increases, but \( I \) decreases and vice-versa. The idea is that the current compensates for a change in the
resistance's value, making $V_{SW}$ almost constant. The gain of the current mirror is chosen such that $V_{SW}$ is set to 1.2V. Also from chapter 3, the gain of the current mirror, $m$, should be kept as small as possible to limit the effect of the noise in the biasing circuit on the phase noise.

4.3 Noise study of delay chain.

To study the noise in the delay line we note from figure 4.2 that there are different loadings on some of the delay stages. Node Phi4 is only loaded by the next differential stage, node Phi2 is loaded by the next differential stage and a level-shifter and node Phi5 is only loaded by a level-shifter. Most nodes are similar to Phi4 (eighteen out of twenty). To do the noise calculations, the ISFs for these three different nodes types need to be computed.

4.3.1 Impulse Sensitivity Functions.

Using the Hajimiri model [6] the chain of delay element configured as an oscillator is studied. The ISFs for the three different nodes Phi2, Phi4 and Phi5 were obtained by simulation using three different methods. First, the ISF for each node is obtained using equation (2.35). The method of the first derivative (equation (2.36)) was then used. Finally, the ISF was approximated as two triangles. The rms and dc values were obtained and are shown in table 4.1. For clarity equation (2.35) and equation (2.36) are repeated next:

$$\Gamma(x) = \frac{f_i'(x)}{\sum_{j \in l} f_j^2(x)}$$

$$\Gamma(x) = \frac{f_i'(x)}{f_{i_{\text{max}}}^2(x)}$$
The direct method (using current pulses) was not used as the estimated simulation times, (2 to 3 weeks), for this method were too long to be practical. In chapter 3 it was shown that the derivative method gave similar results to the direct method and only required a single simulation. It was important however to have confidence in the accuracy of the result and for this reason, the three approximate methods, defined by equation (4.9), equation (4.10) and the triangle were used. To see the difference between the closed form method represented by equation (4.9), and its simplification, equation (4.10), the derivative of the 20 nodes are computed from the steady state solution of the oscillator. These were then used to compute the sum of the derivatives squared for equation (4.9) and this was then compared to the result obtained by using the maximum derivative squared (as required for equation (4.10)). These quantities along with the derivatives are shown in figure 4.12.

As can be seen, equation (4.9) will include the 1/f noise since the asymmetry of the waveform is taken into account. The method defined by equation (4.10) should lead to approximately the same results for the white noise part. The phase noise was computed using the three methods.

Figure 4.13 shows the ISF for node Phi2 using the three methods. Overall, the three methods lead to more or less the same results.
Figure 4.12: Plot of the 20 derivatives, the sum of their squared value and the maximum value of one derivative square.

Figure 4.13: ISF for node Phi2 of the delay chain.

Figure 4.14 shows the ISF for node Phi4. The symmetry criterion is relatively well respected again.
Figure 4.14: ISF for node Phi4 of the delay chain.

Figure 4.15 shows the ISF for node Phi5. The symmetry criteria are also well respected. Note the difference between the closed form method and the derivative method due to the approximation.

Figure 4.15: ISF for node Phi5 of the delay chain.
The first conclusion from the results in table 4.1 is that the symmetry criterion defined by $\Gamma_{dc}$ is reasonably well respected. As can be seen, the dc values are close to 0. The result of this is that the $1/f$ noise present in the delay stage will not be strongly up-converted into close-in phase noise. This is important since this noise is the main reason for phase drift in a low refresh rate frequency synthesiser. Secondly, the differences between the rms and dc values for the different ISFs are significant enough to be taken into account when calculating the phase noise spectrum. In other words, it is not possible to assume that all the nodes have the same ISF. With these results, it is now possible to compute the contribution of each node to the phase noise in the $1/f^2$ region using equation (2.32). The $1/f^3$ region will be obtained using equation (2.35).

4.3.2 Phase noise spectrum.

Taking into account that node Phi2 is loaded by a differential element and a level shifter, equation (2.32) in this case is written as:
\[ L_{\text{Phi}2}(\Delta \omega)_{\text{white}} = \left( \frac{i_n^2 \left( \Gamma \right)_{\text{max}}}{\Delta f} \right) \frac{1}{2(q_{\text{max}} + q_{\text{level}})^2 \Delta \omega^2} \]  

(4.11)

Node Phi4 is loaded by the next differential element, therefore:

\[ L_{\text{Phi}4}(\Delta \omega)_{\text{white}} = \left( \frac{i_n^2 \left( \Gamma \right)_{\text{max}}}{\Delta f} \right) \frac{1}{2q_{\text{max}}^2 \Delta \omega^2} \]  

(4.12)

Taking into account that node Phi5 is loaded only by a level shifter, equation (2.32) in this case is written as:

\[ L_{\text{Phi}5}(\Delta \omega)_{\text{white}} = \left( \frac{i_n^2 \left( \Gamma \right)_{\text{max}}}{\Delta f} \right) \frac{1}{2q_{\text{level}}^2 \Delta \omega^2} \]  

(4.13)

With:

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\frac{i_n^2}{\Delta f})</td>
<td>White noise current density</td>
<td>(1.0126 \times 10^{-23} \text{A}^2/\text{Hz})</td>
</tr>
<tr>
<td>(q_{\text{max}})</td>
<td>Maximum charge due to capacitance load between two differential elements</td>
<td>(200.07 \text{fC})</td>
</tr>
<tr>
<td>(q_{\text{level}})</td>
<td>Maximum charge due to capacitance load between a differential stage and a level shifter.</td>
<td>(44.96 \text{fC})</td>
</tr>
<tr>
<td>(\Delta \omega)</td>
<td>Offset from carrier in radian per second</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.2: Phase noise parameters.
Considering zero correlation between the nodes, the results are added to obtain the total phase noise spectrum. They are 36 nodes similar to Phi4, two similar to Phi2 and two similar to Phi5:

\[
L_w = 10 \log_{10} \left[ 2L_{\Phi 2}(\Delta \omega)_{\text{white}} + 36L_{\Phi 4}(\Delta \omega)_{\text{white}} + 2L_{\Phi 5}(\Delta \omega)_{\text{white}} \right] \quad [\text{dBc/Hz}] \quad (4.14)
\]

This equation represents the phase noise for frequencies higher than the 1/f corner frequency 18.3kHz, (the frequency below which the spectrum is dominated by 1/f noise). This value was obtained by equating equation (4.14) and (4.16) and solving for \( \omega \). The noise corner frequency of a single delay element was simulated to be 792kHz. Thus the 1/f noise dominates the noise delay up to 792kHz. It might also be expected that phase noise corner frequency should be around 792KHz but the actual corner for the phase noise is below this by a factor of forty. This reduction is explained by the fact that low frequency noise, such as device noise, is weighted by the dc coefficient of the ISF's Fourier series, \( c_0 \), which is close to zero due to equal rise time and fall time. Higher frequency noises (white noise) are weighted by the other Fourier series coefficients which are non zero. This in effect “raises” the 1/f^2 region leading to a smaller 1/f^3 corner frequency than the 1/f corner frequency of the delay unit. This is shown in figure 4.16 where the up-converted device noise is shown in black, while down-converted higher frequency noises are shown in red and the resulting phase noise spectrum is shown in blue.

Using equation (4.14) and the parameters of the ISF obtained using the three different techniques (table 4.1) the white phase noise spectra are plotted on figure 4.17. The errors involved using the different methods are shown for this structure. Table 4.3 compares the value of the phase noise of three data points in the 1/f^2 region using the three different techniques.
Figure 4.16: Phase noise corner frequency, $\omega_{\text{ref}}^3$ compared to device noise corner frequency $\omega_{\text{ref}}$ [12].

<table>
<thead>
<tr>
<th>Offset</th>
<th>Closed form method</th>
<th>$1^{\text{st}}$ derivative</th>
<th>Triangle method</th>
</tr>
</thead>
<tbody>
<tr>
<td>20kHz</td>
<td>-83.32dBc/Hz</td>
<td>-87.27dBc/Hz</td>
<td>-74.72dBc/Hz</td>
</tr>
<tr>
<td>100kHz</td>
<td>-97.3dBc/Hz</td>
<td>-101.25dBc/Hz</td>
<td>-88.7dBc/Hz</td>
</tr>
<tr>
<td>1MHz</td>
<td>-117.3dBc/Hz</td>
<td>-121.25dBc/Hz</td>
<td>-108.7dBc/Hz</td>
</tr>
</tbody>
</table>

Table 4.3: Simulated phase noise at different offsets.
According to the model, the first column of table 4.3 should give the most accurate results. In what follows, the simulated phase noise in the $1/f^2$ region due to the VCDL is assumed to correspond to this model.

Using equation (2.35) in the same way equation (2.32) was used, the phase noise spectrum in the $1/f^3$ region is now defined as follows:

\[
L_{\phi 2}(\Delta \omega)_{1/f} = \left( \frac{i^2 c_0^2 \Phi_2}{\Delta f} \right) \frac{\omega_{1/f}}{8(q_{\text{max}} + q_{\text{level}})^2 \Delta \omega^2} 
\] (4.15)

\[
L_{\phi 4}(\Delta \omega)_{1/f} = \left( \frac{i^2 c_0^2 \Phi_4}{\Delta f} \right) \frac{\omega_{1/f}}{8q_{\text{max}}^2 \Delta \omega^3} 
\] (4.16)

\[
L_{\phi 6}(\Delta \omega)_{1/f} = \left( \frac{i^2 c_0^2 \Phi_6}{\Delta f} \right) \frac{\omega_{1/f}}{8q_{\text{level}}^2 \Delta \omega^3} 
\] (4.17)

The full spectrum in the $1/f^3$ region is given by:

\[
L_{1n} = 10 \log_{10} \left[ 2L_{\phi 2}(\Delta \omega)_{1/f} + 36L_{\phi 4}(\Delta \omega)_{1/f} + 2L_{\phi 6}(\Delta \omega)_{1/f} \right] \quad [\text{dBc/Hz}] 
\] (4.18)

Adding the two spectra gives the overall phase noise spectrum as shown on figure 4.18 (solid line). Note again that this is the total phase noise for the device using the open loop swing regulation scheme because this scheme contributes so little to the $1/f$ noise.
4.3.3 Phase noise differences.

At this stage the phase noise due to the VCDL and the phase noise due to the OTA are known and fully defined. Thus, the overall phase noise for a device biased using the replica-biasing scheme can be predicted. Again, assuming zero correlation between the OTA noise and the VCDL noise superposition applies. The total phase noise spectrum for a VCDL biased using the replica biasing is the sum of the phase noise spectrum obtained for the VCDL alone (figure 4.18, solid line) and the phase noise due to the OTA alone, figure 4.10. This is represented in figure 4.18 by the dashed line.

The effect of the OTA is clearly seen with most of the 1/f noise in the spectrum being due to the noise from the amplifier on the control node.

![Figure 4.18: Compared theoretical phase noise for VCO/VCDL using a replica-biasing scheme (dashed line) and an open loop scheme (solid line) to set the voltage swing.](image)

4.4 Stability.

Because the system is a basically a DLL the following linear model applies if the DLL bandwidth is much less than the frequency of the reference signal (chapter 2):
This model does not predict stability limits very accurately. In [2] a new model to predict the stability of a DLL was introduced. It is based on recursive equations describing the error between the inputs of the Phase/Frequency Detector:

$$e(n) = e_0 \left(1 - K_{\text{Loop}}^n\right)$$

(4.20)

Where the error of the $n^{\text{th}}$ edge comparison $e(n)$ is given as a function of the initial error $e_0$. $K_{\text{Loop}}$ is the loop gain and is defined as the product of the charge-pump current times the gain of the delay chain divided by the value of the filter's capacitor.

Four cases are considered depending on the value of the loop gain:

- $0 < \left(1 - K_{\text{Loop}}\right) < 1$ the loop is stable, convergence without overshoot. The system is equivalent to a first order system, equation (4.19).
- $\left(1 - K_{\text{Loop}}\right) = 0$ the loop is stable, locking in one period.
- $-1 < \left(1 - K_{\text{Loop}}\right) < 0$ the loop is stable, damped oscillations converging toward 0.
- $\left(1 - K_{\text{Loop}}\right) \leq -1$ the loop is unstable.

From the above cases it is clear that the loop gain should have a value between 0 and 1 to avoid instability. The gain of the VCDL is given by:

$$K_{\text{DL}} = \frac{2NMd_t}{dV_{\text{ctrl}}} \quad [\text{s/V}] \quad (4.21)$$

Because the gain of the delay chain is fixed by the design, four parameters will affect the stability of the loop: the value of the capacitor, the charge pump current, the input frequency and the feedback ratio. For given values of the
capacitor and charge pump current, values of the input frequency and the feedback ratio can be found to make the loop unstable.

The VCDL gain for the device without a replica-biasing, $K_{dl}$, is found from simulation to be $25\mu s/Volt$. For the device with the replica-biasing the gain is lower: $15.3\mu s/Volt$. With the charge-pump current set at $5\mu A$ the stability versus capacitance and input frequency can be investigated. Figure 4.19 shows the value of $K_{\text{loop}}$ for a capacitor of 400pF and 80pF as the input frequency varies. From this, the loop is unstable for values of input frequencies lower than 40kHz if the capacitor is 80pF.

With these considerations and a nominal input frequency of 48kHz for a feedback ratio of 576, the value for $C$ was chosen to be 400pF. This gives a value for $K_{\text{loop}} = 0.3125$, a value which will ensure stability over process and temperature variations. Hence the system locks without overshoot and can be approximated as a first order system.

![Figure 4.19: Stability limits of the loop versus input frequency for two values of the capacitor.](image)

As a general guide in designing these loops the capacitor is chosen to produce a stable system. Normally the loop bandwidth is kept as wide as possible. This is done to suppress intrinsic device noise components of the device up to the bandwidth of the loop. In PLLs, a large narrow band filter helps in reducing
reference feedthrough which produces detrimental reference spurs around the carrier in the spectrum [9]. The video application for which this device is designed has a high quality clock source and thus the bandwidth of a PLL loop can be increased without the worry of clock feedthrough. With the factorial architecture, however, all input clock noise is fed directly to the output but with the use of a low noise video clock this is not a problem.

4.5 Closed loop phase noise spectrum.

All the elements of the loop are now defined and the overall phase noise spectrum can be obtained. The phase noise of the delay line configured as a VCO is placed in the linear model loop. The transfer function from the output of the delay line to the output was shown to be (chapter 2):

\[
H(s) = \frac{1}{1 + G(s)}
\]

With \( G(s) = \frac{K_{\text{Loop}}}{sT_{\text{ref}}} \) \( K_{\text{Loop}} = \frac{I_{\text{cp}}K_{\text{DL}}}{C} \) (4.22)

After few steps, the squared magnitude of \( H(s) \) has the form:

\[
|H(f)|^2 = \frac{f^2}{f^2 + f_c^2}
\] (4.23)

Where \( f_c \) is equal to the bandwidth of the loop, which was chosen to be 2.8kHz to comply with continuous time domain approximation (bandwidth < a tenth of the input frequency, in this case 32kHz) [10]. This simplifies the analysis of the system. In the white noise region, \( S_{\text{VCDL}}(f) \) can be expressed as:
Where $k_{\text{noise}}$ is a constant obtained using the Hajimiri model, equation (4.14), and has a value of 1.86. Combining equation (2.15) with equation (4.23) and equation (4.24) the output phase noise of the closed loop system is given by:

$$S_\phi(f) = \frac{k_{\text{noise}}}{f^2} \quad [\text{rad}^2/\text{Hz}] \quad (4.25)$$

For frequencies much higher than the bandwidth, equation (4.25) reduces to:

$$S_\phi(f) \equiv \frac{k_{\text{noise}}}{f^2} \quad \text{for } f \gg f_c \quad [\text{rad}^2/\text{Hz}] \quad (4.26)$$

Therefore, for frequencies much higher than the bandwidth, the system's phase noise is equal to the delay line's phase noise in VCO mode. For frequencies within the bandwidth of the system, $S_\phi^{\text{VCDL}}(f)$ corresponds to the $1/f^3$ region, therefore it can be expressed as:

$$S_\phi^{\text{VCDL}}(f) = \frac{k_{1/f}}{f^3} \quad [\text{rad}^2/\text{Hz}] \quad (4.27)$$

Where $k_{1/f}$ is a constant obtained using the Hajimiri. Combining equation (2.15) with equation (4.23) and equation (4.27) the output phase noise of the closed loop system is given by:

$$S_\phi(f) = \frac{k_{1/f}}{f^3 + f^2c^2} \quad [\text{rad}^2/\text{Hz}] \quad (4.28)$$

For frequencies much higher than the bandwidth, equation (4.28) reduces to:
This has a slope of $-10\text{dB/dec}$ below the bandwidth. For frequencies between 2.8kHz, (bandwidth), and 18.3kHz (noise corner frequency) the spectrum corresponds to $1/f$ noise and has a slope of $-30\text{dB/decade}$.

The delay line’s phase noise spectrum, $|H(f)|^2$ in dB and the closed loop phase noise spectra are plotted on figure 4.20.

![Closed Loop Phase Noise Spectrum](image.png)

**Figure 4.20:** Closed Loop phase noise spectrum (solid thick line), $10\log|H(f)|^2$ (dashed line) and open loop phase noise (solid thin line).

Similarly, the closed-loop phase noise spectrum of the VCDL using the replica-biasing can be obtained. Noting that from 0 to 1MHz, the output phase noise of the VCDL is mainly due to the $1/f$ noise (figure 4.18) at the output of the OTA, it can be written as:

$$S_{\phi}^{\text{VCDL}}(f) = \frac{k_{\text{ota}}}{f^3} \quad [\text{rad}^2/\text{Hz}] \quad (4.30)$$
Again combining equation (2.15) with equation (4.23) and equation (4.30) the output phase noise of the closed loop system is given by:

\[ S_\phi(f) = \frac{k_{\text{ota}}}{f(f^2 + f_c^2)} \]  

[rad^2/Hz]  \hspace{1cm} (4.31)

For \( f \ll f_c \), equation (4.31) becomes:

\[ S_\phi(f) \equiv \frac{1}{f} \left( \frac{k_{\text{ota}}}{f_c^2} \right) \]  

for \( f \ll f_c \)  \hspace{1cm} (4.32)

Hence for frequencies smaller than the bandwidth, the slope of the spectrum is -10dB/decade. For frequencies over 1MHz, the VCDL output phase noise is given by equation (4.24) and hence the closed loop phase noise is given by equation (4.25). Between the bandwidth and 1MHz, the spectrum has a slope of -30dB/decade, denoting 1/f noise.

The next figure shows the open loop and closed loop phase noise spectrum for the two systems. The phase noise for the VCDL using the replica-biasing is shown with dashed lines and the phase noise for the VCDL using the optimised biasing is shown with solid lines.

This figure clearly shows that the 1/f noise of the OTA affects the phase noise spectrum of the overall synthesiser for frequencies within the bandwidth of the system. For frequencies higher than the bandwidth the phase noise is white for both synthesisers. These closed-loop plots show that, in order to minimise the effect of the 1/f noise, the bandwidth should be as large as possible; this can achieved by reducing the capacitor's value. The upper bound is defined by the stability of the loop.
4.6 Estimated drift.

In [11] it was experimentally shown that the jitter standard deviation $\sigma_{\Delta T}$ grows as the squared root of the time of observation $T_{\text{obs}}$. This was demonstrated in [12].

$$\sigma_{\Delta T} = \kappa \sqrt{T_{\text{obs}}} \quad [s] \quad (4.33)$$

Where $\kappa$ is a constant related to the thermal noise. If $T_{\text{obs}}$ is long enough then the $1/f$ noise will be dominant and the standard deviation is proportional to the time of observation $T_{\text{obs}}$ rather than to the square root of $T_{\text{obs}}$ [6], [13]. This equation will allow estimation of the phase drift in an open-loop oscillator.
The phase drift can be computed using equation (4.33) with the constant \( \kappa \) given by [13]:

\[
\kappa = \sqrt{\frac{8kT}{3\eta I_{\text{tail}}}} \left( \frac{\gamma}{E_c I_{\text{eff}}^0} + \frac{1}{R_{\text{VCR}} I_{\text{tail}}} \right) \quad [\text{Vs}] \quad (4.34)
\]

Where \( \eta \) is a proportionality constant relating the delay through a stage to the rise and fall time and has a value of 0.9 for differential stages [8], \( \kappa \) has a value of \( 12.62 \times 10^{-9} \text{ Vs} \). The drift will be minimum after a phase reset and will increase in time to reach its maximum just before the next phase reset. The time interval between two phase resets is equal to a reference cycle. For a 48kHz input clock, the drift will be maximum after 20.83\( \mu \)s and has a standard deviation \( \sigma_{\Delta T} = 57.61 \text{ps} \). Taking the 1/f noise into account will increase this value. This done by integrating the phase noise spectrum using equation (2.32), which results in \( \sigma_{\Delta T} = 80 \text{ps} \).

4.7 Additional Circuitry.

4.7.1 Window signal block.

The circuit and the corresponding waveforms are shown in figure 4.22 (a) and (b). Rising edges of \( \Phi_2 \text{level}_n \) are detected and used to reset an S-R latch. Rising edges of the output of the divider are detected and “ANDed” with the reset signal to produce the set signal for the S-R latch. This delays the set signal with respect to the reset signal. The latch output \( Q \) is then set at the end of the count sequence and reset after a duration equal to one period of \( \Phi_2 \text{level}_n \). \( Q \) is finally “ANDed” with a delayed version of \( \Phi_2 \text{level}_n \) to produce the correct signal S1.

In order to insure the SR latch is correctly set and reset over temperature and process variations, a minimum pulse width must be maintained. The duration of the pulse is set by the delay in the edge detector while the start is
determined by the path through the inverter. The pulses can be as wide as half the period of Phi2leveln.

4.7.2 Input Switches.

The system is not implemented with switches as in figure 4.1 (a) but uses digital gates to perform the switching action. The basic idea used is that a 1 or a 0 on one input of a two input NAND gate will allow or impede the value on the other input to pass to the output of the gate. The window signal S1 is used to gate the output clock, Phi5, and the reference signal, CLK_REF. If S1 is high, a new reference edge is allowed in and a phase comparison must be performed. If S1 is low, the output signal is allowed in and no phase comparison is performed. Therefore, S1 also gates Phi5 (Phi5level) before it is input to the variable input (feedback clock) of the PFD. The circuit which accomplishes this is shown in figure 4.23.

![Circuit Diagram](image)

Figure 4.22: Circuit to generate the phase comparison window.
4.7.3 Start Up and delay balancing.

At the beginning, the control voltage node is at 0V. With this condition the delay elements have infinite delay so they neither propagate an input edge, nor oscillate. This means that the circuit must begin by pumping current into the filter’s capacitor such that the voltage reaches the threshold voltage of the delay elements.

Fortunately the PFD detects the incoming clock and notes the absence of a feedback clock and it generates an UP pulse which causes the charge pump to charge up. This UP pulse will be reset only when a falling edge on the variable input of the PFD occurs, i.e. once the circuit produces the $M^{th}$ edge on the
feedback clock. Therefore, the system starts by charging up the filter capacitor to the active range of the delay lines which allows a subsequent lock. Delay mismatch between the PFD REF and VAR inputs (figure 4.24) is critical since any mismatch will lead to fluctuation in the control node. Since the feedback clock PHI5LEVEL is gated by S1, one gate delay is introduced on the VAR path. This delay must be matched on the REF path; hence the insertion of gate G1 in the REF path.

4.8 Conclusion.

The design for a frequency synthesiser with low phase noise and hence low jitter and drift was introduced. The sources of noise in the most critical part of the device, namely the chain of delay elements, were identified and quantified using equations introduced in chapter 2. The delay elements were also designed to have equal rise and fall times to suppress the up-conversion of low frequencies. It was shown that the traditional replica biasing circuit used to set the voltage swing in the VCDL added significantly to the delay line noise at low frequencies. Because of this another bias circuit referred to as an “open loop scheme” was designed. Two versions of the synthesiser were designed: one using a replica-biasing and the other using an open loop regulation scheme. They were fabricated on TSMC’s standard 0.25μm CMOS process. Measurements from these devices were made to compare with the modelling in this chapter and to investigate the theory regarding the negative performance impact of the replica-biasing scheme. The measurements are discussed in the next chapter.
4.9 References.


CHAPTER 5

Practical results and comparison with theory

5.0 Introduction.

The circuits described in chapter 4 were fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) on its 0.25μm standard CMOS process. Different versions of the design were implemented on the same die in order to verify the a priori performances. The relative performances of each version are measured and compared in the time domain and in the frequency domain. In the time domain, the drift is measured and compared with the estimated drift computed in chapter 4. The phase noise estimates are also compared against measurements obtained from the test chip.

During the measurements a phenomenon turned up which was not immediately explained by the model. This phenomenon is investigated in this chapter and then explained.

The test equipment used in the evaluation included sampling oscilloscopes, time interval analysers (TIA), low jitter clock sources and clean power supplies. A low jitter clock source is essential for a DLL based-synthesiser because the input jitter directly appears at the output (chapter 2). Power supply noise will also produce output jitter, so it is important to begin with clean supplies and add a predefined amount of noise at a prescribed frequency to evaluate the effect of supply noise. Finally it is important to design the PCB carefully adding appropriate de-coupling where necessary.

Results in the time domain (jitter) shown in this chapter were obtained using a WAVECREST DTS2077 [1] and an HP54120B [2] digitising oscilloscope. Phase noise results were obtained using an Anritsu MS2661C [3] spectrum analyser and an HP4395A [2] network analyser.
5.1 The die.

Before discussing the results, the contents of the testchip are introduced. A photo-micrograph of this chip is shown in figure 5.1. This chip contains different versions of the fractional DLLs. These components are labelled in figure 5.1 and the differences between the implementations are described in table 5.1.

![Figure 5.1: The 4 fractional DLLs implemented on chip. From top to bottom: FDLL1, FDLL2, FDLL3 and FDLL4. On the right hand-side are the multiply by 4 PLLs.](image)

<table>
<thead>
<tr>
<th>FDLL1</th>
<th>Uses a replica-biasing scheme to regulate the voltage swing in the chain of delay elements. It has a fixed divider ratio of 576 and a PLL connected to its output.</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDLL2</td>
<td>Is similar to FDLL1 except that it uses the “open loop” voltage swing regulation scheme. It has a fixed divider ratio of 576, and a PLL connected to its output.</td>
</tr>
<tr>
<td>FDLL3</td>
<td>Is similar to FDLL2, except that it attains lock configured as a PLL. Once in lock, it switches back to FDLL mode.</td>
</tr>
<tr>
<td>FDLL4</td>
<td>Is similar to FDLL2 except it has a programmable filter and divider.</td>
</tr>
</tbody>
</table>

Table 5.1: Description of different FDLL implementations on the test chip.
A detailed layout of FDLL4 is shown on figure 5.2. The different parts to the circuit are highlighted.

![Figure 5.2: FDLL4 layout.](image)

To avoid cross-talk, each synthesiser was designed with a "sleep" input. This turns off all transistors in the synthesisers which are not in use and thus the only noise sources present arise from the device under test.

### 5.2 Phase drift.

The most important and difficult synthesiser parameter for the target video applications is the phase drift of the clock. Because of the large number of output clock cycles generated between input clock edges, there is significant opportunity to accumulate drift. All design efforts were concentrated on reducing this drift. Drift is measured as the uncertainty of the time elapsed between a reference clock edge, and any of the output clock edges. Figure 5.3 helps with the explanation. The drift increases in time as was shown in chapter 4 by equation (4.31), it will be minimum just after an input clock edge where the
phase drift is essentially reset, and maximum just before the next incoming edge. Since the time duration between two refresh instants is defined by the duration of one reference clock cycle, the maximum drift will occur $T_{ref}$ seconds after the first refresh. The maximum drift results will now be introduced in section 5.2.1 and then section 5.2.2 reports on the manner in which the drift accumulates over time.

![Diagram showing how to measure drift.](image)

**5.2.1 Maximum drift.**

Figure 5.4 is a histogram which is a representation of the maximum drift obtained from FDLL4 (no-replica biasing, no-output PLL). The input signal's frequency is 48kHz and the multiplication is 584 (28MHz output clock). The maximum drift then is the variation of the time started by an input clock edge and ended after 584 edges of the output clock (just before the next phase reset incoming clock). The peak to peak value of the histogram is 840ps.

For comparison, figure 1.4, in chapter 1 showed the same measurement for a PLL designed for the same process. This PLL had a reference clock twice as fast (100kHz instead of 48KHz) and a smaller multiplication factor (256). The measured drift however was ten times larger than the one measured for the FDLL4 (8.78ns instead of 0.84ns). This measurement validates the choice of architecture.
The same measurement was performed for the circuit using the replica-biasing based voltage swing scheme with an input frequency of 48kHz. The divider here has a fixed value of 576. The result is shown on figure 5.5. Note the peak to peak value of the histogram is 7.308ns. This confirms the harmful effect of the OTA on the system’s performance as was postulated in chapter 4.

Figure 5.4: Clock drift of the 4th FDLL, no replica-biasing.

Figure 5.5: Clock drift of the 1st FDLL, with replica-biasing.
5.2.2 Accumulation.

If the drift measurement is repeated for several edges the growth of the drift with increasing time from the input clock edge can be investigated. Figure 5.6 shows the build up in drift as the output edges are more delayed from the input clock. The measure of drift plotted in figure 5.6 is the rms value of the variation or $\sigma$ of the associated Gaussian distribution. With the arrival of the new clock edge the phase is once again reset. The fact that the uncertainty does not reset to 0 at those instants is due to a low frequency noise component in the measurement system which accumulates over the 22$\mu$s [4]. The FDLL structure itself resets the phase to zero.

Plotting the data of figure 5.6 on a Log-Log plot makes it possible to identify the nature of the noise sources in the system. In chapter 4, it was shown that the jitter standard deviation increases as the square root of the time of observation, $\tau$ (equation 4.31), in case of white noise. On a Log-Log scale, this will appear as a straight line with a slope of 0.5 ($\log_{10}(\sqrt{x}) = 0.5\log_{10}(x)$). In [4], it is shown that 1/f noise will also appear as a straight line but with a slope of 1. This is shown on figure 5.7 where just after a phase reset the phase noise is dominated by white noise (slope of 0.5). This continues up to 6$\mu$s. After this the noise is dominated by the 1/f noise (slope of 1) and this continues up to the next phase reset.

![Figure 5.6: Jitter accumulation.](image)
Fitting a line to the data on figure 5.7 allows the computation of a value for $\kappa$ (see equation 4.32 chapter 4) of $15.1 \times 10^{-9} \sqrt{s}$. This compares well to the calculated value of $12.3 \times 10^{-9} \sqrt{s}$.

5.3 Peak to peak jitter.

Peak to peak jitter is perhaps the most common type of measurement used to characterise the quality of a clock signal. The measurement consists of measuring the variations in the duration of the clock's period over a large number of non-adjacent periods. Recording the longest and the shortest periods in the process and subtracting them the peak to peak value is obtained. The number of samples taken depends on the required level of confidence. As an example when testing a SONET system, the test must be done over 10,000 periods.

In the FDLL, the peak to peak jitter is also a measure of the drift since the last period before refresh will be extended or reduced by the drift term. Thus it is probable that the longest and shortest period will be a period which occurs just
before refresh. Figure 5.8 shows how the drift directly modulates the last period before refresh.

![Diagram showing drift modulation](image)

*Figure 5.8: Peak to peak jitter as drift.*

Figure 5.9 compares the peak to peak jitter of a two Factorial DLLs as the input frequency is increased. The blue line plots the data from the FDDL using replica-biasing scheme. The red line shows the results for the FDDL with the “open loop” swing regulation scheme. As was stated the swing regulation was the only difference between the two circuits, in fact the chain of delay elements are identical. They both have a fixed multiplication ratio of 576. The two devices are connected (on-chip) to a multiply-by-4 PLL, bringing the multiplication ratio to 2304. Both devices were designed for a nominal input frequency of 48kHz.

From figure 5.9 it is obvious that the output noise of the OTA significantly degrades performance. The jitter has improved by a factor of five. It should be noted that the best performance for the device without replica is obtained for a 48kHz input. Figure 5.9 also shows how the device copes with slightly altered input frequencies. It is important that it maintains its performance from 35kHz to
60kHz. This shows that the architecture would be robust in volume production where processing can significantly change bias levels in the device.

Figure 5.9: Effect of replica-biasing on jitter. Top curve: using a replica-biasing scheme; bottom curve: using an optimised bias circuit.

Figure 5.10 shows how the drift varies as the input frequency changes. For this measurement FDLL4 is used. The output frequency is maintained to 28MHz. The changing input frequency is accommodated with a programmable divider. As can be seen, for a 48kHz input clock the peak to peak jitter is 0.84ns which is what was measured for the drift on the same device with the same settings (figure 5.4).

The increase in jitter at low frequency is explained by the fact the bandwidth of the synthesiser is proportional to the input frequency. Reducing the bandwidth increases the noise because the loop will not reject as much noise. Inspecting figure 5.10 the shapes suggests 1/f noise. If the noise is 1/f noise it can be expressed as:

\[ N_{1/f} \propto \frac{1}{f} \]  

(5.1)
In this case the output frequency is kept at 28MHz thus the input frequency is inversely proportional to the feedback divider $N_{fb}$. Therefore the noise can be expressed as:

$$N_{1/f} \propto N_{fb}$$  \hspace{1cm} (5.2)

Thus, plotting the drift data of figure 5.10 versus the feedback ratio should produce a straight line if the noise is dominated by $1/f$ noise. This is shown in figure 5.11.

The linear dependence of the deviation on the feedback divider ($N_{FB}$) allows for prediction for higher feedback ratio (lower input frequency). In figure 5.11 such a prediction is done for a feedback ratio of 1877, corresponding to an input frequency of 15kHz. The drift predicted is 1.4ns. This figure compares well to results obtained in [5], 1.6ns for an input frequency of 150kHz. In other words this architecture achieves the result obtained in [5] with an input frequency which is a factor of ten below that used in [5]. The 15kHz input frequency is also significant in so far as it represents a lower limit for the target video applications.
The results on figure 5.11 further agree with the measurements of the variation versus observation time shown in figure 5.7. The straight line section with a slope of one in figure 5.7 denotes 1/f noise. All of this data in figure 5.11 corresponds to this section of the data in figure 5.7. Figure 5.7 shows that thermal noise dominates up to 6ns after the refresh cycle. All input clock periods in figure 5.11 are longer than this.

Figure 5.12 compares drift for two bandwidth settings. The different bandwidth settings are achieved by changing the filter capacitor from 80pF to 360pF. As can be seen the increased bandwidth setting (80pF) is beneficial. Again, the peak to peak deviation is linearly dependent on the feedback ratio, changing the bandwidth with the filter capacitor changes the slope of the line.
Figure 5.12: Bandwidth influence over drift.

Period jitter is usually characterised by histogramming a large number of measured periods. The HP54120B oscilloscope has a feature which automatically produces this histogram and the parameters of the associated Gaussian model. This measurement for FDLL4 is shown on figure 5.13:

Figure 5.13: Jitter on an HP54120B digitising scope.

Figure 5.13 shows the position of the clock edges. To obtain this picture, an edge of the output is displayed on screen. The persistence of the oscilloscope is ON in order to "see" the position of each edge. If the histogram is examined, most of the periods have a similar duration. This is also seen with the thickness
of the defined clock edge. As well as this cluster of edges there is clearly an infrequent occurrence of shorter periods to the left of this. These periods correspond to the last period before the incoming clock edge.

5.4 Spectral content of clock.

The measurements shown so far have shown the time domain performance of the clock. Phase noise measurements are presented and compared with the theoretical values computed in chapter 4. From these measurements estimates of bandwidth can also be compared with predictions. The reference clock feed-through is also assessed from the spurs in the phase noise measurements.

5.4.1 Phase noise spectrum.

Figure 5.14 shows the phase noise results obtained for FDLL4 with an input frequency of 48kHz, a multiplication ratio of 576 and a value of 400pF for the filter’s capacitor. The solid line is the simulated phase noise spectrum (closed form method), the dashed line represents the measurements. The model and the measurements agree well. Table 5.2 compares simulated results presented in table 4.3 and some of the phase noise data points measured with the spectrum analyser.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Phase noise:</th>
<th>Phase noise:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Closed form method</td>
<td>measured</td>
</tr>
<tr>
<td>10kHz</td>
<td>-83.32dBc/Hz</td>
<td>-77.88dBc/Hz</td>
</tr>
<tr>
<td>100kHz</td>
<td>-97.3dBc/Hz</td>
<td>-99.5dBc/Hz</td>
</tr>
<tr>
<td>1MHz</td>
<td>-117.3dBc/Hz</td>
<td>-116.5dBc/Hz</td>
</tr>
</tbody>
</table>

Table 5.2: Simulated phase noise vs measured phase noise at different offsets.
The errors at an offset of 10kHz can be explained by the fact this frequency represents the lowest offset frequency measurable by the spectrum analyser so the measurement accuracy is questionable.

Overall there is a good agreement between the theoretical and measured phase noise spectra, especially at high offset frequencies. For frequencies offsets over 18.3kHz from the carrier, the phase noise of the system was predicted to be white, which is the case as the measured slope is roughly 20dB/decade.

### 5.4.2 Bandwidth.

The bandwidth of the system was computed to be 2.8kHz (chapter 4, section 4.5). Using a narrow resolution bandwidth (10Hz or even 3Hz) on the spectrum analyser, it is possible to measure it. This is shown on figure 5.16 where the measured bandwidth (taken from the shoulder of the phase noise, chapter 2) is approximately equal to 1.4kHz. This value is lower than the designed value but there is a tolerance on the designed bandwidth because of process variations. The component tolerances on the components are as follows:

- Capacitor: ±7%
- Charge-pump current: ±25%
• Gain of the VCDL: ±30%

These tolerances were computed from simulation using the worst case models. The tolerances listed above result in a tolerance of ± 70% on the bandwidth and this explains the discrepancy. The bandwidth was measured using the HP4395A network analyser.

Figure 5.15: Measurement of the device bandwidth using the power spectrum $S_v(f)$.

### 5.4.3 Spurs.

Spurs appear on the spectrum at multiples of the reference clock. Seen in figure 5.16 they suggest a deterministic error occurring at the reference frequency. The first spur is 85.6 dB below the carrier which contributes 0.428ps to the jitter assuming ideal spectral component (chapter 2).
5.5 Static phase offset problem.

When the data in figure 5.13 is examined, it is seen that the mean value of the last periods before refresh are slightly less than the average of the other cycles. This agrees with the spectral rays seen in figure 5.16. It was explained in section 5.3 that the last cycle is lengthened or shortened by the drift which occurs over an input clock period. If this was the only phenomenon at work the average of the last cycle would be the same as that of all other cycles. Looking at figure 5.17, which is a histogram of all cycles, it is seen that all the "last" cycles appear to the left hand-side of the peak of the histogram. A WAVECREST DTS2077 recorded this data.
When this phenomenon was measured, a number of detailed simulations were carried out to see where this offset was coming from. It became clear that the charge pump was responsible for the offset. Charge-pump simulations were run to analyse the problem. The PFD and charge pump were stimulated with a reference clock and a variable input clock of the same frequency but the phase offset between the two signals was set to ±500ps. Figure 5.18 (a) shows the basic structure. The theoretical response is shown on figure 5.18 (b) where a phase delay on the variable input clock causes the current $I_{UP}$ to flow into the capacitor for a duration of 500ps which will cause $V_C$ (the filter/capacitor voltage) to increase (red lines figure 5.18). For a delay of −500ps, it will cause the current $I_{DN}$ to flow off the capacitor causing the voltage across the capacitor to decrease (blue lines figure 5.18). If the charge-pump was perfect, the increase and decrease in the control voltage would be symmetrical around the initial value of $V_C$, figure 5.18 (b). However, this is not the case and the actual situation is depicted on figure 5.18 (c). This simulation is repeated with different initial values of $V_C$ and the results are shown on figure 5.19. In this chart the increase or decrease in $V_C$, $\Delta V$, is plotted versus the delay between the reference and the variable clock. As can be seen in the figure the charge-pump does not respond symmetrically to symmetrical phase errors. For the different
starting voltages on \( V_c \) the input clocks must be offset by different amounts to stop the charging of the capacitor. This phase offset versus starting filter voltage is plotted on figure 5.20. There are four possible reasons for this asymmetry. The first option concerns the fact that once in lock the PFD produces small up and down pulses of equal width, thus no net charge is added to the capacitor and the control voltage stays constant. Any significant mismatch between the width of these pulse widths would charge the capacitor up or down. As the widths of the up and down pulses are fixed by a chain of matched inverters, they can not be significantly different. Secondly, the same problem can arise if there was a delay mismatch in the signal path to the reference and feedback input to the PFD. This is not the case (chapter 4, section 4.7.2). This was verified by simulation. A third possible cause of mismatch lies in the current sources \( I_{UP} \) and \( I_{DN} \) providing currents of different absolute values. This hypothesis is also rejected since the current sources are based on mirroring of the same initial current. The absolute values can not be significantly different. The fourth possibility is a charge-dumping problem. When the switches open or close they add or remove charge to or from the capacitor. If the N and P channel devices which make up the up down switches dump different amounts of charge with each switching then there will be a net charge deposited on the filter capacitor during every refresh event. This charge is balanced by the device control loop by forcing a phase offset at the PFD input. This charge mismatch will change with the filter voltage because the P-channel switch capacitor is referenced to \( V_{DD} \) while the N-channel switch capacitance is referenced to ground.
Figure 5.18: Charge-pump static offset.

Figure 5.19: Voltage change in the filter's voltage after 100 cycles vs. the phase offset between the REF and VAR clock for different starting filter voltages.
5.5. Power supply noise rejection.

If the device is to be integrated on a chip it is essential that it performs well even in the presence of supply noise. This noise can be produced by digital switching on the chip. To test the robustness of the architecture a 100mV peak-to-peak sine wave ac coupled to the DC supply voltage of the chip. The output clock jitter was then recorded as the frequency of this sine wave was changed. From figure 5.21 it is seen that the jitter peaks as the VDD noise frequency reaches the bandwidth of the loop. This happens because it is at this frequency that the movement caused by the VDD change can accumulate in one direction for most of a reference cycle thus greatly enhancing the drift in the device. For higher frequencies the drift cause by a positive or negative VDD swing will accumulate for a small fraction of the cycle before it is cancelled by the subsequent swing of the reverse polarity. For very low frequencies only a small amount of the VDD cycle will be seen by each input clock cycle and thus the negative effects are minimised by the control loop. The open loop sensitivity for the delay unit was estimated at 0.18%/Volt. These measurements assert that the device rejects VDD noise well.
5.6. Stability range.

The stability (device able to gain lock) of the device was computed in chapter 4 for different values of the filter’s capacitor with a range of input frequencies. These computations were tested using FDLL4, which has a programmable capacitor and a programmable feedback counter. The following table compares the predicted stability versus the actual stability for two values of the capacitor versus input frequency.

<table>
<thead>
<tr>
<th>Input frequency (kHz)</th>
<th>C=80pF</th>
<th>C=400pF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Predicted</td>
<td>Actual</td>
</tr>
<tr>
<td>28</td>
<td>Unstable</td>
<td>Unstable</td>
</tr>
<tr>
<td>30</td>
<td>Unstable</td>
<td>Unstable</td>
</tr>
<tr>
<td>35</td>
<td>Unstable</td>
<td>Unstable</td>
</tr>
<tr>
<td>40</td>
<td>Stable</td>
<td>Unstable</td>
</tr>
<tr>
<td>Over 40</td>
<td>Stable</td>
<td>Stable</td>
</tr>
</tbody>
</table>

Table 5.3: Stability, actual versus theory.
In table 5.3, it is seen that for an input frequency of 40kHz and a capacitor of 80pF, the device is theoretically stable while in practice it is not. In figure 4.19, these values of input frequency and capacitor are shown to give a marginally stable system. Any variations in the value $K_{\text{loop}}$ due to process variations will cause the device to go into the unstable region as seen on the measurements.

5.7. Conclusion.

The FDLL designed in chapter 4 works as expected. The results from a test chip reported in this chapter validate the approach taken to obtain a low drift synthesiser. The replacement of the replica-biasing scheme by an optimised regulation scheme led to significant improvements in terms of drift as expected from chapter 4 (figure 5.4 and figure 5.5). The model used to predict the FDLL phase noise proved to be correct (figure 5.14). An unexpected static phase offset problem in the charge-pump circuit was measured, investigated and understood. VDD rejection characteristics of the device were measured and it proved robust in the presence of significant VDD noise. Finally the stability model for the device was investigated and it proved accurate.

5.8. Reference.


6.1 Summary.

Chapter 1 introduces two types of television screens: the Cathode Ray Tube and Flat screens (based on liquid crystal or Plasma). How the picture is displayed on screen is briefly explained. It describes a video signal and how it is used in a CRT to obtain an image. It explains how flat panels screens require digital data to reproduce an image and because of this the video signals need to be digitised. The digitisation process requires the generation of a stable sampling clock from the horizontal synchronisation pulse in the video signal. This pulse occurs at a low frequency (tens of kHz) while the sampling clock needs to be of much higher frequency (up to couple of hundreds of MHz). Thus the focus of this thesis was introduced, that is to produce a quality high frequency clock from the low frequency synchronisation pulse in a video signal.

Chapter 2 gives theoretical background on noise in PLLs and DLLs. It begins by discussing a sinusoidal voltage, which is phase-modulated, and introduces expressions which explain phase noise and how this relates to spectral power. A suitable phase noise model by Hajimiri is then explained which allows the estimation of phase noise in oscillators. Finally this chapter shows how PLL and DLL control loops modify the open loop oscillator phase noise.

In chapter 3, three different oscillator topologies are investigated and designed. All three produce the same frequency and consume roughly the same power. The Hajimiri model is used to obtain the simulated phase noise spectra of these
three oscillators. The results show that the single-ended oscillator with variable capacitor outperforms the two other topologies. Further simulations show that common mode noise has significant impact on all but the differential oscillator and this is then proposed as the preferred architecture for integration.

In chapter 4 Fractional Delay-Locked Loop (FDLL) synthesisers are explained. The design of this circuit is shown in detail. From the results obtained in chapter 3, a differential topology is chosen because of the noisy target application. During the design a major source of low frequency noise is identified and an architecture modification is introduced to limit the effects on the overall drift in the device. Different versions of the FDLL were designed to investigate whether the modification to the architecture was successful or not.

Chapter 5 presents practical results obtained from the chip designed in chapter 4. The results agree with the design values of chapter 4. In particular, it is shown that the circuit modification to reduce low frequency noise improved the drift parameter by a factor of four.

6.2 Conclusions.

6.2.1 Comparison of CMOS Oscillator topologies.

Chapter 3 compared three oscillator topologies in terms of their relative phase noise. They were designed for the same output frequency (111MHz) and roughly the same power (2mW). Their a priori phase noise spectra were estimated using the Hajimiri model (direct method). This has led to the first conclusion that a single-ended oscillator with voltage controlled capacitor loads significantly outperforms the two other commonly used topologies, a single ended Current Starved ring oscillator and a differential ring oscillator. This is only a partial conclusion however since the Hajimiri model does not include supply or substrate noise. By modelling these noise sources in simulations and examining the oscillator's responses, it was shown that the two single-ended
oscillators are very sensitive to this supply and substrate noise. The best circuit for rejecting supply and substrate noise is shown to be the differential oscillator, as expected. The differential structure was more robust by a factor of 10 to 30 over the single ended structures. For this reason, the final conclusion of chapter 3 was that the differential topology is best suited for the target video application.

6.2.2 New low drift synthesiser configuration.

In Chapter 4 a new configuration for a low drift synthesizer was introduced. This configuration used the idea of making an oscillator to interpolate between refresh cycles. This idea was also used in previous work but the manner in which it was realised was different. The design described also allowed for programmable options. The effective feedback divider was variable between 4 and 1024. The bandwidth of the loop was variable through the addition of a variable filter capacitor.

6.2.3 Analysis and optimisation of synthesiser components.

All components used in the design were analysed. The noise sources present in the chain of delay elements as well as the noise introduced by the bias circuits was studied and phase noise predictions were produced for all designs using the Hajimiri model. A commonly used “replica biasing” scheme was seen to introduce significant 1/f noise into the circuit. To reduce this noise an “open loop” regulation scheme was designed. To confirm the projected improvements of the “open loop” scheme both schemes were designed and implemented.

6.2.4 Results from testchip.

Phase noise predictions were measured and compared to the predictions of the Hajimiri model. The predictions were accurate to within 1dBc/Hz@1MHz.
A number of other design parameters were confirmed to be close to the designed values. These included bandwidth, stability and VDD rejection. The programmability in the structures allowed examination of the operation of the device over a wide range of input frequencies. This allowed investigation of the noise spectrum of the VCO. The key design parameter, drift, was measured for the FDLL with the "replica" and "open loop" biasing schemes. The optimised regulation scheme improved the drift by a factor of eight over the "replica" biasing scheme which again agreed with theory.

6.2.5 Drift performance.

The resulting drift from this architecture is totally compatible with the requirements of a range of video standards. The work shows an improvement of a factor of 6 over a recently reported architecture.

6.2.6 Summary of research outcomes.

The key outcomes of this work are as follows:

- a new synthesiser architecture was introduced which minimises phase noise re-circulation in the device and thus reduces drift.
- techniques used in the design of RF synthesisers were applied to video clock synthesisers and this allowed optimisation of the synthesiser components and a redesign of standard biasing blocks
- the drift results from the optimised synthesiser block implemented as part of this research are the best reported to date.
6.3 Further work.

The single-ended oscillator with variable capacitors has shown very good performance in terms of phase noise, as shown in chapter 3. If it was not for a high sensitivity to supply and substrate noise, this structure might perform very well. The sensitivity to supply noise can be overcome by designing a regulated power supply. The addition of "deep nwell" technology which would protect the structure from substrate noise should be investigated further [1]. The structure might then be very attractive for this application and would warrant consideration.

If the architecture presented in this thesis is used as a starting point, three changes might improve its performance. The first change would involve increasing the feedback divider to achieve multiplication factors over 2000. This is straightforward but would involve decreasing the effective delay in the delay line to increase the FDLL output frequency. This reduced delay might have more inherent 1/f noise but the overall structure might perform better than the cascaded FDLL and PLL. Another change would again involve increasing the multiplication ratio without a cascaded PLL. The idea here would be to logically combine the multiple phases available in the chain of delay elements. A multiplication by four for example would not require much logic (<10 gates) and thus would not degrade the performance of the device.

A final way to improve the performance of the FDLL in this thesis can be appreciated by referring to figure 5.9. In figure 5.9 the drift parameter is plotted against output frequency. It shows that there is a narrow range of frequencies for which the drift is low. The reason that the drift increases beyond this range is that the Hajimiri rise fall time criterion is not maintained. The improvement to the FDLL would involve moving this narrow range of frequencies as shown by the blue line in the simplified picture of Figure 6.1. Here the blue line which is centred at fc1 is shifted and re-centred at fc1 or fc0.
Figure 6.1: Shifting the minimum deviation around the input frequency.

This is achieved by adding (removing) capacitors at each node of the delay chain. This forces the device to remain at a voltage for which the Hajimiri criterion is maintained. In fact the added capacitors in this circuit act as a coarse tuning mechanism for the frequency and the voltage controlled resistors of the delay element fine tune the frequency. This is shown on figure 6.2.

Figure 6.2: Adding capacitors to coarse tune the delay.
This method requires additional logic circuitry to select the appropriate capacitors. This decoding to drive the capacitor's switches could be done with the control bits typically used to select the video standard (different frequencies) being used. This feature should supply a FDLL that is effectively centred in the low drift region for all of the video standards. This addition should not only improve the average performance but it would also make the performance robust over process and temperature.

6.4 Reference.

Appendix A

Integrating phase noise

An example of phase noise integration is given here. The phase noise power is then put in the context of a 110MHz clock to obtain a jitter figure. The data in table A.1 give phase noise in dBc/Hz at a given offset frequency from the carrier.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Phase noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100kHz</td>
<td>-89.3</td>
</tr>
<tr>
<td>1MHz</td>
<td>-115.6</td>
</tr>
<tr>
<td>10MHz</td>
<td>-136.4</td>
</tr>
<tr>
<td>20MHz</td>
<td>-141</td>
</tr>
<tr>
<td>30MHz</td>
<td>-142.9</td>
</tr>
</tbody>
</table>

Table A.1: Phase noise data.

The corresponding phase noise $S_\phi(f)$ is plotted in figure A.1:

Figure A.1: Phase noise plot of free running oscillator simulation, $S_\phi(f)$. 
Because the phase noise is given as dBc/Hz it must be converted to power assuming a 0dBm reference level or 1 milliwatt according to:

\[ S_e(f) = 0.001 \times 10^{\frac{\text{dBc}}{10}} \]  

(A.1)

The equation given by Egan can now be used to integrate to phase noise power in a piecewise manner. For instance between frequency \( f_1=100\text{kHz} \) and \( f_2=1\text{MHz} \), the slope \( \alpha \) is 3 since the slope in dBc is approximately equal to \(-30\text{dB/decade} \). The phase noise power at \( f_1=100\text{kHz} \), using equation (A.1), is \( 1.1749 \times 10^{-12} \text{mW} \). Therefore the phase noise power in the bandwidth 100kHz-1MHz is:

\[
p_1 = \int_{100 \times 10^3}^{1 \times 10^6} S_e(f)df = \frac{100 \times 10^3}{3+1} \times 1.1749 \times 10^{-12} \times \left[ \left( \frac{1 \times 10^6}{100 \times 10^3} \right)^{3+1} - 1 \right] = 5.8157 \times 10^{-8} \]

(A.2)

And so:

\[
p_2 = \int_{1 \times 10^6}^{10 \times 10^6} S_e(f)df = 2.48 \times 10^{-9} \]

(A.3)

\[
p_3 = \int_{10 \times 10^6}^{20 \times 10^6} S_e(f)df = 1.1454 \times 10^{-10} \]

(A.4)

\[
p_4 = \int_{20 \times 10^6}^{30 \times 10^6} S_e(f)df = 6.41 \times 10^{-11} \]

(A.5)

Adding these four partial powers will give the total phase noise power:

\[
p_t = p_1 + p_2 + p_3 + p_4 = 6.082 \times 10^{-8} \]

(A.6)

A.2
Treating this sideband number as a phase modulation allows the computation of a jitter figure. Converting the phase noise power $p_T$ into dBm assuming a reference level of $0\text{dBm}$ gives:

$$\text{dBm} = 10 \log_{10} \left( \frac{p_T}{0.001} \right) = -42.16$$  \hspace{1cm} (A.7)

The timing jitter is then:

$$J_{\text{rms}} = \frac{10^{\text{dBm}/20}}{2\pi f_{\text{osc}}}$$  \hspace{1cm} (A.8)

In the case of an oscillation frequency $f_{\text{osc}}$ of $110\text{MHz}$, the rms jitter $J_{\text{rms}}$ is $11.28\text{ps}$. 

A.3
Appendix B
Test board

Figure B. 1 shows the test board designed to test the circuits. It includes filters to clean the different supply voltages. Each part of the integrated is supplied by its own pair of VDD and GROUND. This is to avoid any noise coupling that might occur between input and output pads. Also visible on figure B.1 are the switches to change the feedback divider and the filter's components.

Figure B.1: Test board.