Analysis and Synthesis of Primary Side Cycle by Cycle Control of Isolated Flyback Converters

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Analysis and Synthesis of Primary Side Cycle by Cycle Control of Isolated Flyback Converters

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Analysis and Synthesis of Primary Side Cycle by Cycle Control of Isolated Flyback Converters

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Submitted in partial fulfilment for the Degree of Doctor of Philosophy

The work presents the analysis and design of an isolated flyback converter, without feedback from the load side. The converter is controlled from the primary side using the switch voltage and transresistance control circuitry.

A detailed study of the flyback converter dynamics, including all known perturbations. Besides the standard parasitic components, resistive effect, other parasitic effects are included in the model such as inter coil coupling, source capacitance, etc. Discussion about circuit simplifications with a focus on the design of this model development, it is possible to control the output voltage and to control the circuit performance.

The output voltage of the isolated flyback converter is controlled on the primary side provides the information about the input limitation and is used in each switching cycle. A novel control mechanism based on the digital implementation of information provides primary side cycle by cycle feedback to the flyback converter. With the control mechanism, different power conversion modes are possible in the same circuit, this extends the range of the converter load operations.

The control methodology is theoretically and experimentally verified. Variable frequency modulation is used to control the converter and the proposed control strategy is validated using real-time experiments. During the start-up, they are designed to provide the output voltage, characteristics, and the number of possible control modes are verified. The control scheme is adjustable for different types of power systems.

Signature of Author:

Certified by: Dr. N. Barry

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Abstract

This work presents the analysis and design of an isolated flyback converter, without feedback from the load side. The converter is controlled from the primary side using the switch voltage and innovative control circuit topologies.

A detail study of the flyback circuit is undertaken including all known parasitics. Besides the standard parasitics, for example the capacitor resistive effect, other more subtle effects are included in the model development such as inter coil coupling, source capacitance etc. Development of these models has provided information about circuit simplifications without losing accuracy of the model. As a consequence of this model development, it is possible to accurately calculate the load voltage from the switch voltage and to control the circuit performance.

The output voltage of the isolated flyback converter calculated on the primary side provides the load control information in each switching cycle, without the traditional feedback loop and the use of an opto-coupler to isolate the feedback signal. The information about the input line is also updated in each switching cycle. A novel control mechanism based on the line and the load regulation information provides primary side cycle by cycle voltage mode control of the flyback converter. With the control mechanism continuous, conduction mode and discontinuous conduction mode are possible in the same circuit, this extends the range of the converter load operations.

The control methodology is theoretically and experimentally verified. Variable frequency modulation is used in the power control with both variable on-time and variable off-time. The methodology can also be extended to Electromagnetic Interference (EMI) sensitive applications where a constant switching frequency is desirable.

The circuits proposed and discussed in this work have their own dedicated start-up circuits. During the start-up they operate in current mode control to provide the shortest start-up times possible. The start-up circuits use a limited number of components suitable for incorporation into an integrated solution.
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List of Symbols

\( V_{in} \) the DC input voltage [V]
\( v_{in} \) the input voltage [V]
\( V_o \) the DC output voltage [V]
\( v_o \) the output voltage [V]
\( v_{oon} \) the output voltage of a flyback converter during the on-time interval [V]
\( v_{ooff} \) the output voltage of a flyback converter during the off-time interval [V]
\( v_{oc} \) the output voltage of a flyback converter calculated on the primary side during the off-time [V]
\( v_{Lmon} \) the primary side inductor voltage during the on-time interval [V]
\( v_{Lmoff} \) the primary side inductor voltage during the off-time interval [V]
\( V_{SW} \) the DC primary side switch voltage [V]
\( v_{SW} \) the primary side switch voltage [V]
\( V_F \) the forward voltage drop of a diode dictated by \( v_F = f(i_F) \) [V]
\( v_F \) the forward voltage drop of the output diode if a flyback converter [V]
\( V_{CON} \) voltage of the output capacitor, \( C \), during the on-time interval [V]
\( V_{Co}(0) \) voltage the initial condition of \( C \) during the on-time interval [V]
\( V_{Coff}(0) \) voltage the initial condition of \( C \) during the off-time interval [V]
\( V_{esr} \) voltage across the esr [V]
\( i_{in} \) input current of a flyback converter [A]
\( i_{Lmon} \) magnetising current during the on-time interval [A]
\( i_{Lmon}(0) \) current the initial condition of \( i_{Lmon} \) [A]
\( i_{Lmon}(E) \) current \( i_{Lmon} \) at the end of the on-time [A]
\( i_{Lmoff} \) magnetising current during the off-time interval [A]
\( i_{Lmoff}(0) \) current the initial condition of \( i_{Lmoff} \) [A]
\( i_{soff} \) the secondary side current during the off-time [A]
\( i_{soff}(0) \) the initial condition of the secondary side current [A]
\( i_{CON} \) current of the output capacitor, \( C \), during the on-time interval [A]
\( i_{Coff} \) current of the output capacitor, \( C \), during the off-time interval [A]
\( i_{oon} \) the output current of a flyback converter during the on-time interval [A]
\( i_{ooff} \) the output current of a flyback converter during the off-time interval [A]
\( L_s \) the secondary side inductance of a flyback converter [H]
\( L_m \) the magnetising inductance of a flyback converter [H]
\( N_P \) number of primary turns of a flyback transformer
\( N_S \) number of secondary turns of a flyback transformer
\( R \) the load resistance [\( \Omega \)]
\( C \) or \( C_o \) the output capacitor [F]
\( esr \) equivalent serial resistance of the output capacitor [\( \Omega \)]
\( P_{out} \) the output power of a converter [W]
\( P_{loss} \) the total power loss of a converter [W]
\( \eta \) the efficiency of a converter [%]
$R_T$  the total thermal resistance [W/K]  
$T_s$  temperature of the uniform surface of a converter – a box [K]  
$T_a$  the ambient temperature [K]  
$A$  the surface area of a power supply [m^2]  
$h$  the heat transfer coefficient [W/(m^2*K)]  

$T_s$  switching period [s]  
$t$  time [s]  
$t_{on}$  the on-time [s]  
$t_{offCCM}$  the off-time during continuous conduction mode [s]  
$t_{offDCM}$  the off-time during discontinuous conduction mode [s]  
$t_0$  time at which $i_{soff}$ reaches zero [s]  

$X$  DC value in the time domain  
$x$  x(t)  
$\bar{x}$  AC signal perturbation  
$s$  Laplace domain  
$X(s)$  x(t) value in Laplace domain  
$X(0)$  the initial condition of x(t)  
$X(E)$  the end condition of x(t)  
$CCM$  continuous conduction mode index  
$DCM$  discontinuous conduction mode index
Chapter 1
Introduction

Nowadays numerous electronic devices enable us to live our daily lives. The products of the modern science era have become indispensable parts of everyday life. Their presence in all the areas of human existence gives them the status of essential components, as a consequence the area of electronics is growing rapidly along with competition in the field.

In the diversity of electronic equipment there is one element present in all of them, it is a power supply, which converts applied input power into a desired output power. In most cases it is an AC/DC or a DC/DC converter and these power converters are not basic diode rectifiers but sophisticated switch mode power supplies. These devices have to meet many demands and requirements, for example:

- Safety aspects,
- Materials,
- EMC,
- Local (continental) markets
- Industrial specifications
- Environmental

Despite all these regulations the power electronics market is growing fast. The analysts project that AC/DC power supplies, the largest part of the market, will grow from $9.1 billion in 1999 to approximately $12.2 billion in 2004 and that DC/DC will grow from about $3 billion in 1999 to almost $5 billion in 2004 [www.darnell.com]. These projections are for the global commercial market.

This thesis is concerned with DC/DC isolated converters and more specifically the flyback converter. The isolation is mainly in the interest of safety to insure that there is a path from any one terminal to the ground. It also allows a positive with respect to a negative terminal to be provided, similar to a battery. The safety requirements have been quantified over the years by many agencies throughout the world [G4].
Another important aspect of this work is to address the following trends in modern electronics, when studying the flyback converter, namely:

- Size reduction
  - Packaging
  - Integrated Magnetics
- Good dynamic performance
  - High bandwidth control loops
- High power density
  - High operation temperature
- Cost reduction
  - Low number of components
  - Simple manufacture process

This thesis is directly orientated on two of the mentioned aspects, namely: Fast control loops and high operation temperature. Indirectly it has an impact on all the aspects of modern electronics.

1.1 Power density versus temperature of operation and efficiency.

The trend is to reduce down the size of DC/DC converters for the expanding markets in mobile phones, portable computers and other handheld devices. Packaging of the power devices becomes critical in this event and the power density per unit is important. In the case of galvanically isolated outputs, opto-couplers are often used in the feedback path, in preference to signal transformer or capacitive coupling, § 4.1. However opto-couplers have a serious degradation problem with temperature and time, showing in some cases a halving of the expected lifetime when the junction temperature increases by as little as 10°C. The fundamental reason for this problem is due to a reduction in the light output from the LED (due to recombination current) at higher junction temperatures [E7]. The opto-coupler also exhibits a high degree of non-
linearity in its current transfer ratio, CTR, and choosing the operating point is critical. With the use of opto-couplers other components are required to set the operating point and to filter high frequency noise [A2]. There is also mechanical stress consideration to be taken into account with the design of opto-couplers [E7] and the resulting stress, which the power supply can be subjected to. For integrated packaged isolated switch mode power supplies these problems are even further exacerbated, especially the ageing problem with high temperature operation. Switches and diodes have ratings normally up to 160°C for their junction temperatures. Opto-couplers’ performance begins to roll off at junction temperatures as low as 30°C.

The reason why we want to operate at high temperature is explained below. The power loss, $P_{loss}$, of a converter module is given as:

$$P_{loss} = P_{out} \left( \frac{1}{\eta} - 1 \right) \quad (1.1)$$

where: $\eta$ is the efficiency and $P_{out}$ is the power output. The power is also given as [G8]

$$P_{loss} = R(T_s - T_a) = Ah(T_s - T_a) \quad (1.2)$$

where $R$ is the thermal resistance. $T_s$ is the surface temperature of the converter module. $T_a$ is the ambient temperature in K. $A$ is the surface area of the power module in $m^2$ and $h$ is the heat transfer coefficient in $\frac{W}{m^2 K}$. If we assume that $h$, $A$ and $T_a$ are constant and if $T_s$ goes up then $P_{loss}$ in Eq.2 also rises up. As a consequence the efficiency is constant and independent of temperature, Eq.3.

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \quad (1.3)$$

A higher loss is possible at a higher surface temperature, $T_s$. We see from the equations above that the power module surface temperature can go to a higher temperature to give the higher power loss. Alternatively the surface area can be reduced if the power module can operate at a higher surface temperature, giving a consequential
volume saving to the power module. Eliminating the opto-coupler will help with achieving this.
Chapter 2
Review of Isolated Converters

Use of a transformer in DC-DC converters allows isolation and multiple outputs. It also can lead to better conversion optimisation when very large or very small conversion ratio are required [G1]. By proper choice of the transformer turns ratios, the voltage or current stresses imposed on the transistors and diodes can be minimised, leading to improved efficiency and lower cost.

There are several ways of incorporating transformer isolation into a DC-DC converter. The full-bridge, half-bridge, forward and push-pull converters are commonly used isolated versions of the buck converter. The flyback converter is an isolated version of the buck-boost converter. In this paragraph we analyse with details the flyback topology and briefly review forward and half-bridge topologies as middle range power converters.

2.1 Flyback converter

The flyback converter is derived from the buck-boost converter. Steps in the derivation are shown in Fig.2.1. The basic buck-boost converter, Fig.2.1a, contains a switching component, $Q1$, an inductor, $L$, a diode, $D$, and the output capacitor, $C$. In Fig.2.1b, the inductor winding is made of two parallel wires, with 1:1 turns ratio. The basic function of the inductor is unchanged. When the inductor windings are separated, Fig.2.1c, then we have the flyback topology with negative output voltage. In this case $L_m$ is the magnetising inductance (primary side inductance) and $L_s$ is the secondary side inductance. $L_s$ can be expressed by Eq.2.1.

$$L_s = L_m \left( \frac{N_s}{N_p} \right)^2$$  \hspace{1cm} (2.1)

When the switch $Q1$ is on, then current flows through the primary winding, $N_p$. The secondary side current flows through the secondary winding, $N_s$ and the diode, $D$, when $Q1$ is off. Although the two-winding magnetic component is represented by the same
symbol as for the transformer, it is more precise to call it a “two-winding inductor” or a “flyback transformer”. If the flyback transformer polarity is reversed, Fig.2.1d, then the flyback converter with positive output voltage is obtained.

Fig. 2.1: The flyback converter derivation: a) buck-boost converter; b) inductor $L$ is wound with two parallel wires; c) separated inductor windings – the flyback converter with negative output, d) the flyback converter with positive output.
2.1.1 Accurate solution in s-domain and in the time-domain for CCM

The flyback transformer in Fig. 2.1d can be replaced by an equivalent circuit, see Fig. 2.2. The magnetising inductance, \( L_m \), is referred to the transformer's primary side. The model assumes perfect coupling between windings and neglects losses. The switch is realised using a MOSFET. The MOSFET is assumed to be an ideal switch, with \( R_{on}=0 \) (resistance during the on-time). When the switch conducts, Fig. 2.2b, energy from the DC source, \( V_{in} \), is stored in \( L_m \). When the diode conducts, Fig. 2.2c, the stored energy is transferred to the load. The inductor voltage, \( v_{L_m} \), and current \( i_{L_m} \) are scaled according to the transformer turn ratio.

To find an accurate solution for the output voltage, \( v_o \), of the converter it is necessary to include the equivalent serial resistance, \( esr \), of the output capacitor. Initial conditions also have to be taken into account. The final solution for \( v_o \) will consist of two parts. (1) for the on-time interval, when the MOSFET conducts and the second (2) for the off-time interval, when the output diode, \( D \), conducts. To find the final solution we have decided to construct equations in the Laplace domain. Maple® mathematical software was used to solve the equations and to find the inverse Laplace transform.

During the on-time, in CCM, the complemented circuit from Fig. 2.2b is shown in Fig. 2.3. The circuit is constructed in s-domain and contains initial conditions, \( V_{Con}(0) \) and \( I_{Lmon}(0) \). Partial equations are derived in time domain.

On the primary side, input current, \( i_{in} \), and the inductor voltage, \( v_{Lmon} \), are given by

\[
\begin{align*}
i_{in} &= i_{Lmon} \quad (2.2) \\
v_{Lmon} &= V_{in} \quad (2.3)
\end{align*}
\]

The inductor current \( i_{L_m} \) is expressed by

\[
i_{Lmon} = I_{Lmon}(0) + \frac{1}{L_m} \cdot \int V_{in} dt \quad (2.4)
\]
Fig. 2.2: Flyback converter circuit: a) with transformer equivalent model; b) during the Q1 on-time; c) during the off-time, CCM.
On the secondary side the output current, $i_{oon}$, and the output voltage, $v_{oon}$, are given by

$$i_{oon} = -i_{Con}$$  \hspace{1cm} (2.5) $$v_{oon} = v_{esr} + v_{Con}$$  \hspace{1cm} (2.6) 

Once we know the output capacitor current the output voltage can be found. Expanding Eq.2.6 we obtain an expression with $i_{Con}$ only, Eq.2.7.

$$-i_{Con} \cdot R = i_{Con} \cdot esr + \frac{1}{C} \cdot \int i_{Con} \, dt + V_{Con}(0)$$  \hspace{1cm} (2.7) 

In Eq.2.7 $V_{Con}(0)$ is the initial condition equal to the capacitor voltage at the end of the previous off-time, $V_{CoFF(E)}$. From Eq.2.7 current $i_{Con}$ can be easy calculated. Nevertheless the same solution can be found from Eq.2.8, which is in s-domain. We have decided to do it in this way to keep order, which will help us to go through equations in the off-state of the converter.

![Flyback converter in s-domain during the on-time, including initial conditions.](image)

Fig. 2.3: Flyback converter in s-domain during the on-time, including initial conditions.
\[ I_{on} := -\frac{V_{con0} C}{1 + s C (R + esr)} \]  \hspace{1cm} (2.8)

Eq.2.8 is imported from Maple. \( V_{con0} \) is equivalent to \( V_{con(0)} \) and \( := \) means \( = \). The Maple programming restrictions cause this small difference in description. The solution of Eq.2.8 is found in the s-domain and transformed into the time domain, see Eq.2.9.

\[ icon := -\frac{V_{con0} e^{-\frac{t}{C (R + esr)}}}{R + esr} \]  \hspace{1cm} (2.9)

Hence the output voltage during the on-time is given by

\[ v_{oon} := \frac{V_{con0} e^{-\frac{t}{C (R + esr)}}}{R + esr} \]  \hspace{1cm} (2.10)

Voltage across the output capacitor is given by

\[ v_{con} := V_{con0} e^{-\frac{t}{C (R + esr)}} \]  \hspace{1cm} (2.11)

During the off-time the complemented circuit from Fig.2.2c is shown in Fig.2.4.
Fig. 2.4: Flyback converter in the s-domain during the off-time, including initial conditions.

In this case the input current, $i_{in}$, does not flow in the circuit, Eq.2.12. The primary-side magnetising inductance voltage, $v_{Lmoff}$, is expressed by Eq.2.13. The magnetising current, $i_{Lmoff}$, with the initial condition $I_{Lmoff}(0)$ is expressed by Eq.2.14. The initial condition is equal to the primary side current at the end of the previous on-time, $I_{Lmoff}(0) = I_{Lmon(E)}$. It is important not to mix this current up with the secondary side current of the two-winding inductor. Eq.2.14 is just the Faraday derived equation for the circuit shown in Fig.2.4. In a physical two-winding inductor there is no current flowing on the primary side during the off-time.

$$i_{in} = 0$$  \hspace{1cm} (2.12)

$$v_{Lmoff} = -v_{ooff} \frac{N_p}{N_S}$$  \hspace{1cm} (2.13)

$$i_{Lmoff} = I_{Lmoff}(0) - \frac{1}{L_m} \frac{N_p}{N_S} \int v_{ooff} \, dt$$  \hspace{1cm} (2.14)

The initial condition, $I_{soff}(0)$, of the secondary side current, $i_{soff}$, is
\[ I_{\text{soff}}(0) = I_{\text{Lmon}}(E) \cdot \frac{N_p}{N_S} \quad (2.15) \]

Voltage across the secondary side winding of the flyback transformer is equal to the output voltage of the converter. The secondary side current is

\[ i_{\text{soff}} = I_{\text{soff}}(0) - \frac{1}{L_s} \int v_{\text{soff}} \, dt \quad (2.16) \]

From Kirchoff’s 1st law the output current’s, \( i_{\text{soff}} \), equation can be derived, Eq.2.17, and from Kirchoff’s 2nd law the output voltage, Eq.2.18.

\[ i_{\text{ooff}} = i_{\text{soff}} - i_{\text{coff}} \quad (2.17) \]
\[ v_{\text{ooff}} = v_{\text{esr}} + v_{\text{Coff}} \quad (2.18) \]

Combining Eq.2.16 to Eq.2.18 with basic Ohm’s law equations the secondary side currents can be derived. This is done in s-domain. The output capacitor current, \( I_{\text{coff}}(s) \) denoted \( I_{\text{coff}} \) is given by

\[ I_{\text{coff}} := \frac{-L_s I_{\text{soff}}(0) + s L_s I_{\text{soff}}(0) + R I_{\text{soff}}}{R} \quad (2.19) \]

The secondary side current, \( I_{\text{soff}} \), is given by

\[ I_{\text{soff}} := \frac{-R C V_{\text{coff}}(0) + R C L_s I_{\text{soff}}(0) + s + \text{esr} s C L_s I_{\text{soff}}(0) + L_s I_{\text{soff}}(0)}{\text{esr} s^2 C L_s + \text{esr} s C R + s L_s + R + s^2 L_s R C} \quad (2.20) \]

The solution of Eq.2.20 in time domain is Eq.A1.2.21
Assuming $esr^2=0$, it simplifies to Eq.2.22.

$$i_{off} := \left(\left(4 \omega T2 C R Vcoff0 esr - 2 \omega Ls T2 esr Isoff0 + 2 \omega T2 C R^2 Isoff0 esr + 4 \omega T2 C R^2 Vcoff0 - 2 \omega Ls T2 R Isoff0 \right) \sin(\omega t) \right) \div \left(-2 R T2 esr - 4 R^2 T2 + Ls^2\right)$$

$$+ Isoff0 \cos(\omega t) \right)e^{-\frac{1}{2} \left(\frac{esr C R + Ls}{T2 (esr + R)} \right)t}$$

(2.22)

Where $T2$ and $\omega$ are:

$$T2 = Ls \cdot C$$

(2.23)

$$\omega := \frac{1}{2} \sqrt{-\frac{-4 T2 R^2 - 2 T2 R esr + Ls^2}{T2^2 (R + esr)^2}}$$

(2.24)

Eq.2.22 can be converted into Eq.2.25, shown below.

$$i_{off} = e^{\left(\frac{1}{2} \left(\frac{esr C R + Ls}{T2 (esr + R)} \right)t\right)} \cdot A1 \cdot \sin(\omega \cdot t + \phi l)$$

(2.25)

Where $A1$, $a1$, $b1$ and $\phi l$ are

$$A1 = \sqrt{a1^2 + b1^2}$$

(2.26)

$$al := -2 \omega T2 (2 C R Vcoff0 esr - Ls esr Isoff0 + C R^2 Isoff0 esr + 2 C R^2 Vcoff0 - R Isoff0 Ls)$$

$$2 R T2 esr + 4 R^2 T2 - Ls^2$$

(2.27)

$$b1 := Isoff0$$

(2.28)
\[ \phi_1 = \arctan \left( \frac{b_1}{a_1} \right) \]  \hspace{1cm} (2.29)

Eq.2.25 is as expected and represents the decaying transience.

An accurate solution of Eq.2.19, from Maple, in the time domain is Eq.A1.2.30. Assuming \( esr^2 = 0 \), \( esr^3 = 0 \) and substituting Eq.2.23 with Eq.2.24, simplified form of Eq.A1.2.30 is obtained.

\[ i_{\text{off}} = e^{-\frac{1}{2} \left( \frac{t}{T_2 \left( esr + R \right)} \right)^2} \cdot A_2 \cdot \sin(\omega \cdot t + \phi_2) \]  \hspace{1cm} (2.31)

Where \( A_2 \) is expressed by Eq.2.32, and \( a_2, b_2 \) with \( \phi_2 \) are as shown below.

\[ A_2 = \sqrt{a_2^2 + b_2^2} \]  \hspace{1cm} (2.32)

\begin{align*}
a_2 & := -2 T_2 \omega \left( esr C R^3 L_{\text{off0}} - esr L_{\text{off0}} + 3 esr C V_{\text{off0}} R^3 + esr L_{\text{off0}} - L_s V_{\text{off0}} R \\
& \quad + L_s R^2 L_{\text{off0}} + 2 C R^3 V_{\text{off0}} \right) / \left( 6 T_2 R^2 esr - L_s^2 esr + 4 R^3 T_2 - L_s^2 R \right) \hspace{1cm} (2.33)
\end{align*}

\begin{align*}
b_2 & := \left(-2 esr R T_2 V_{\text{off0}} + 2 esr R^2 L_{\text{off0}} T_2 + V_{\text{off0}} L_s^2 - R L_{\text{off0}} L_s^2 + 4 R^3 L_{\text{off0}} T_2 \\
& \quad - 4 R^2 T_2 V_{\text{off0}} \right) / \left( 6 T_2 R^2 esr - L_s^2 esr + 4 R^3 T_2 - L_s^2 R \right) \hspace{1cm} (2.34)
\end{align*}

\[ \phi_2 = \arctan \left( \frac{b_2}{a_2} \right) \]  \hspace{1cm} (2.35)

Substituting Eq.2.25 and Eq.2.31 into Eq.2.17 the output current during the off-time can be calculated.

\[ i_{\text{off}} = e^{-\frac{1}{2} \left( \frac{t}{T_2 \left( esr + R \right)} \right)^2} \cdot \left[ A_1 \cdot \sin(\omega \cdot t + \phi_1) - A_2 \cdot \sin(\omega \cdot t + \phi_2) \right] \]  \hspace{1cm} (2.36)
Once we have the output current $i_{off}$, the output voltage can be calculated using Ohms law, $v_{off} = R \cdot i_{off}$. Nevertheless Eq.2.37 is derived from accurate equations of the currents, Eq.2.21 and Eq.2.30. It is done in this way to obtain the simplest and the most accurate forms of coefficients in Eq.2.37.

$$v_{off} = e^{-\left(\frac{1}{2} \frac{C \cdot (R + L_s) \cdot t}{T^2} \right)} \cdot A3 \cdot \sin(\omega \cdot t + \phi 3)$$ (2.37)

Where $A3$, $a3$, $b3$ and $\phi 3$ are

$$A3 = \sqrt{(a3^2 + b3^2)}$$ (2.38)

$$a3 := 2 \frac{\omega R T^2 (I_{soff} L_s (R - 2 R - 3 \cdot esr) + V_{coff0} (C R^2 \cdot esr + L_s (R + \cdot esr)))}{Ls^2 (R + esr) - T^2 (4 R^3 + 6 R^2 \cdot esr)}$$ (2.39)

$$b3 := 0$$ (2.40)

$$\phi 3 = \arctan\left(\frac{b3}{a3}\right)$$ (2.41)

In “all” the above final equations we have assumed that $esr^2 = 0$ and $esr^3 = 0$. This assumption has negligible influence on accuracy of the solutions. It is confirmed by comparative analysis of simplified solution for the output voltage, $v_{off}$, Eq.2.37, with accurate solution represented by Eq.A1.2.42. Results are shown in Fig.2.5 and Fig.2.6. These results are only to check accuracy of the solution depending of the simplification made. Values of components and initial conditions are from a simulated circuit presented in Chapter 9. In Fig.2.5 can be seen the output voltage represented by the accurate solution (continuous line) and the simplified solution (points). They are very close together. Encouraged by this result we have tried to go further with simplification.
We assumed additionally $L_s^2=0$, results are shown in Fig. 2.6. Divergence between the accurate solution (continuous line) and the simplified solution (points) is unacceptable.

Fig. 2.5: An accurate solution and a simplified solution ($esr^2=0, esr^3=0$) of $v_{o\text{off}}$.

Fig. 2.6: An accurate solution and a simplified solution ($esr^2=0, esr^3=0, L_s^2=0$) of $v_{o\text{off}}$. 

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Simplified final equations for a flyback converter in CCM, over one operation cycle, can be written as below.

\[
\begin{align*}
V_n &= \begin{cases} 
V_{con}(0) \cdot e^{\left(\frac{-t}{C(R+esr)}\right)} \cdot R & \text{during } t_{on} \\
\frac{R + esr}{e^{\left(\frac{1}{2} \frac{t}{T_2(esr+R)}\right)}} \cdot A_3 \cdot \sin(\omega \cdot t + \phi_3) & \text{during } t_{off}
\end{cases} \\
\end{align*}
\]

(2.43)

\[
\begin{align*}
i_n &= \begin{cases} 
0 & \text{during } t_{on} \\
\frac{1}{2} \frac{t}{T_2(esr+R)} \cdot A_1 \cdot \sin(\omega \cdot t + \phi_1) & \text{during } t_{off}
\end{cases} \\
\end{align*}
\]

(2.44)

\[
\begin{align*}
i_C &= \begin{cases} 
-V_{con}(0) \cdot e^{\left(\frac{-t}{C(R+esr)}\right)} \cdot R & \text{during } t_{on} \\
\frac{R + esr}{e^{\left(\frac{1}{2} \frac{t}{T_2(esr+R)}\right)}} \cdot A_2 \cdot \sin(\omega \cdot t + \phi_2) & \text{during } t_{off}
\end{cases} \\
\end{align*}
\]

(2.45)

Results obtained from Eq.2.43 to Eq.2.45 together with the output current over one complete operation cycle are shown below. Period \(T=4\mu s, t_{on}=1.3\mu s\) – from simulation.
The output voltage of a flyback converter and its average value are shown in Fig. 2.7. Voltage across the output capacitor also is placed in Fig. 2.7. It can be seen that the output voltage steps-up when the switch goes off. This is caused by the directional change in current of the output capacitor, (see Fig. 2.8). This current flows through the
$esr$ and the instant change appears as a step in the output voltage, indirectly in the output current too, see Fig.2.9. The difference between $v_{o_{off}}$ and $v_{C_{off}}$ ($v_{C_{off}}$ derived by the definition from $i_{C_{off}}$) decreases with the secondary side current, $i_{o_{off}}$. When $i_{o_{off}}$ is smaller than the output current then $v_{C_{off}}$ becomes bigger than $v_{o_{off}}$ ($i_{C_{off}}$ changes direction). In Fig.2.7 some discontinuity of $v_{C_{off}}$ can be seen. This is an effect of simplification in the derived equations.

![Graph](image)

Fig. 2.9: Currents of a flyback converter in one complete operation cycle, CCM, simplified equation, $esr=0.005 \Omega$.

The discontinuity does not appear in the capacitor voltage shown in Fig.2.10. These results are from the accurate equations. It is necessary to be aware of the consequences of simplifications in the equations, especially during analysis of cycle by cycle controlled converters. This example also shows the range of the $esr$'s problem in power converters, not only in flyback converters. In Fig.2.7 to Fig.2.10 $esr=0.005 \Omega$. For comparison we show example of $esr=0.001 \Omega$ with simplified equations in Fig.2.11. It can be seen that the $esr$ voltage step is smaller and there is no discontinuity in $v_C$. In this case simplifications are fully justified.
In these analyses the \textit{esl} of the output capacitor was not taken into account. This is also an important issue but in this case the \textit{esr} suffices in the amplitude analysis. We are interested in the output voltage regulation over one complete operation cycle. Instant step change in the output voltage is acceptable in our analysis, once the amplitude is correct.
In case of study of EMC aspects the \( esl \) has to be taken into account together with Printed Wiring Board (PWB) layouts [E21]. The EMI analyses will not be realistic if the PWB layout is excluded [G7].

2.1.2 Accurate solution in s-domain and in the time-domain for DCM

The above analysis is for flyback converters operating in CCM. They can be easily complemented and applied to DCM. Circuits in Fig.2.2b and Fig.2.2c are valid for the first two states of the converter. Only the primary side current’s initial condition in Eq.2.4 is equal to zero because \( i_{\text{off}} \) reaches zero before the end of the off-time (third stage of the converter). A circuit shown in Fig.2.12 represents this third stage. Circuits in the s-domain are shown in Fig.2.13. There is only one initial condition, the output capacitor voltage, \( V_{\text{CDCM}}(0) \). The secondary side of this circuit is the same as in Fig.2.2b. Eq.2.9 to Eq.2.11 and Eq.2.5 can describe voltages and currents, respectively. The only difference is that \( V_{\text{c off}}(0) \) is now equal to the output capacitor voltage at the time when \( i_{\text{off}}=0 \), \( V_{\text{CDCM}}(0) \).

Fig. 2.12: Flyback converter circuit during the off-time in DCM.
Fig. 2.13: Flyback converter in s-domain during the off-time in DCM, including initial condition.

Time, $t_0$, at which $i_{soff}$ reaches zero, can be calculated from Eq.2.48, which is a simplified version $(esr^2=0, T2=Ls^C$ and $\omega)$ of the accurate solution, Eq.A1.2.46.

\[
t_0 := -\frac{\frac{1}{T2 \omega} \left( -V_{coff0}(2 C R^2 + 2 C esr R) + Isoff0 (R Ls - C R^2 esr + Ls esr) \right)}{\arctan \left( \frac{I_{soff0} (-2 R T2 esr - 4 R^2 T2 + Ls^2)}{1 - V_{coff0} (2 C R^2 + 2 C esr R) + Isoff0 (R Ls - C R^2 esr + Ls esr)} \right)}
\]

Substituting Eq.A1.2.46 into the output capacitor voltage during the off time, which is the integration of the capacitor current, $i_{coff}$, we obtain $V_{CDCM(0)}$, Eq.A1.2.47. A simplified version of this equation is Eq.A1.2.49.

The final equations for a flyback converter in DCM, over one operation cycle can be written as below.
\[
\begin{align*}
\text{v}_o &= e^{-\left(\frac{1}{C(R+esr)}\right) \cdot R} \\
&\cdot \left\{ \begin{array}{l}
V_{\text{on}}(0) \cdot e^{-\left(\frac{1}{C(R+esr)}\right) \cdot R} \cdot \frac{1}{R+esr} \quad \text{during} \quad t_{\text{on}} \\
0 \quad \text{during} \quad t_{\text{on}}
\end{array} \right. \\
&\cdot \left\{ \begin{array}{l}
\frac{1}{2} T(\text{est+R}) \cdot A1 \cdot \sin(\omega \cdot t + \phi) \quad \text{during} \quad t_{\text{offDCM}} \\
0 \quad \text{during} \quad t_{\text{offDCM}}
\end{array} \right.
\end{align*}
\]

(2.50)

\[
\begin{align*}
\text{i}_s &= e^{-\left(\frac{1}{C(R+esr)}\right) \cdot R} \\
&\cdot \left\{ \begin{array}{l}
V_{\text{on}}(0) \cdot e^{-\left(\frac{1}{C(R+esr)}\right) \cdot R} \cdot \frac{1}{R+esr} \quad \text{during} \quad t_{\text{on}} \\
0 \quad \text{during} \quad t_{\text{on}}
\end{array} \right. \\
&\cdot \left\{ \begin{array}{l}
\frac{1}{2} T(\text{est+R}) \cdot A1 \cdot \sin(\omega \cdot t + \phi) \quad \text{during} \quad t_{\text{offDCM}} \\
0 \quad \text{during} \quad t_{\text{offDCM}}
\end{array} \right.
\end{align*}
\]

(2.51)

\[
\begin{align*}
\text{i}_c &= e^{-\left(\frac{1}{C(R+esr)}\right) \cdot R} \\
&\cdot \left\{ \begin{array}{l}
V_{\text{on}}(0) \cdot e^{-\left(\frac{1}{C(R+esr)}\right) \cdot R} \cdot \frac{1}{R+esr} \quad \text{during} \quad t_{\text{on}} \\
0 \quad \text{during} \quad t_{\text{on}}
\end{array} \right. \\
&\cdot \left\{ \begin{array}{l}
\frac{1}{2} T(\text{est+R}) \cdot A1 \cdot \sin(\omega \cdot t + \phi) \quad \text{during} \quad t_{\text{offDCM}} \\
0 \quad \text{during} \quad t_{\text{offDCM}}
\end{array} \right.
\end{align*}
\]

(2.52)

Results obtained from Eq.2.50 to Eq.2.52 together with the output current over one complete operation cycle are shown below. Period \( T=4\mu s \) extended from the previous example to reach DCM, \( t_{\text{on}}=1.3\mu s \) – from simulation.
Fig. 2.14: Voltages of a flyback converter in one complete operation cycle, DCM, simplified equations, $esr=0.005\Omega$.

The output voltage with its average value and voltage across the output capacitor in DCM are shown in Fig.2.14. It can be seen that in the first two time intervals (on-time, off-time CCM) waveforms are the same as in Fig.2.7 and can be analysed in the same way. The third time interval (off-time DCM) represents discontinuous conduction mode of the converter. As a result of the equations simplification, some discontinuity in $v_{Coff}$ can be seen (the border between $v_{CoffCCM}$ and $v_{CoffDCM}$). This discontinuity does not appear in the output voltage, $v_{oot}$. And, as in CCM, strongly depends on the value of $esr$, see Fig.2.18 ($esr=0.001\Omega$). The results from not simplified equations are shown in Fig.2.17.

The difference between $v_{ootDCM}$ and $v_{CoffDCM}$ during DCM is now dictated by the ratio $R/(R+esr)$ during the on-time. The secondary side current, $i_{soffDCM}=0$, and the capacitor current, $i_{CoffDCM}$, are shown in Fig.2.15. Current $i_{CoffDCM}$ approaches zero from the negative side with a long time constant, see Eq.2.15.

The output current is shown in Fig.2.16. It can be seen that $i_{ootDCM}$ follows the capacitor current, as during the on-time, according to Eq.2.5.
Fig. 2.15: Currents of a flyback converter in one complete operation cycle, DCM, simplified equations, $esr=0.005\Omega$.

Fig. 2.16: The output current of a flyback converter in one complete operation cycle, CCM, simplified equation, $esr=0.005\Omega$. 
Fig. 2.17: Voltages of a flyback converter in one complete operation cycle, DCM, accurate equations, $esr=0.005 \Omega$.

Fig. 2.18: Voltages of a flyback converter in one complete operation cycle, DCM, simplified equations, $esr=0.001 \Omega$
2.1.3 State-space average models in CCM and DCM

For the design purposes the Bode plots of the converter transfer function are very important, [G1], [G4]. There are two major transfer functions used.

- **The line-to-output transfer function, Eq.2.53.** This is found by setting the duty cycle variation, \( \tilde{d}(s) \) to zero. Then we solve for the small-signal equivalent circuit model of the transfer function, from \( \tilde{v}_m(s) \) to \( \tilde{v}_o(s) \).

  \[
  G_{\text{out}}(s) = \frac{\tilde{v}_o}{\tilde{v}_m|_{\tilde{d}(s)=0}}
  \]  
  
  (2.53)

  This transfer function describes how variations in the input voltage, \( \tilde{v}_m(t) \), lead to disturbances in the output voltage, \( \tilde{v}_o(t) \).

- **The control-to-output transfer function, Eq.2.54.** It is found by setting the input voltage variations, \( \tilde{v}_m(s) \), to zero and then solving the small-signal equivalent circuit model for the transfer function from \( \tilde{v}_o(s) \) as a function of \( \tilde{d}(s) \).

  \[
  G_{\text{cd}}(s) = \frac{\tilde{v}_o}{\tilde{d}|_{\tilde{v}_m(s)=0}}
  \]  
  
  (2.54)

  This transfer function describes how the control input variations, \( \tilde{d}(s) \), influences the output voltage, \( \tilde{v}_o(s) \). This transfer function is a key component of the loop gain and has a significant effect on the regulator performance.

In case of the flyback converters, Eq.2.55 expresses the line-to-output transfer function in CCM.

\[
G_{\text{out}} = -\frac{(R + esr) \ D1}{(esr \ (2 \ D1 - 1) + (-1 + D1) \ R) \ TR}
\]  

(2.55)
Where, \( D1 \) is the on-time, \( t_{on} \), and \( TR \) is the turns ratio of the flyback transformer. When \( esr=0 \), then the widely known expression [G1] is obtained:

\[
G_{in\_esr\_0} = -\frac{D1}{(-1 + D1) TR}
\]  
(2.56)

And Eq.A1.2.57 expresses the control-to-output transfer function in CCM. In Eq.A1.2.57, \( C_o \) is the output capacitor. In case of \( esr=0 \), Eq.A1.2.57 will reduce to:

\[
G_{o\_in\_esr\_0} = \frac{(D1 s \ Lm - 2 \ TR^2 R D1 + TR^2 R D1^2 + TR^2 R) \ Vin}{(s^2 \ Lm R C_o + TR^2 R D1^2 - 2 D1 s \ Lm + TR^2 R + s \ Lm - 2 TR^2 R D1) (-1 + D1)^2 TR}
\]  
(2.58)

In DCM the transfer functions are shown below. \( G_{oin} \) is expressed by Eq.2.59 and by Eq.2.60 when \( esr=0 \).

\[
G_{oin} := \frac{\sqrt{2} \ \sqrt{\frac{Lm}{TR^2 R T_s}} \ TR R T_s \left(2 \ esr \sqrt{2} \ \sqrt{\frac{Lm}{TR^2 R T_s}} - esr + R \right) D1}{-4 \ Lm \ esr + \sqrt{2} \ \sqrt{\frac{Lm}{TR^2 R T_s}} TR^2 \ esr \ T_s R - 2 R Lm}
\]  
(2.59)

\[
G_{oin\_esr\_0} = \frac{1}{2} D1 \sqrt{2} \ \sqrt{\frac{T_s \ R}{Lm}}
\]  
(2.60)

\( G_{od} \) in DCM is expressed by Eq.A1.2.61 and by Eq.2.62 when \( esr=0 \).

\[
G_{od\_esr\_0} := \frac{\sqrt{2} \ \sqrt{\frac{Lm}{TR^2 T_s R}} \ R TR \ Vin \ T_s}{Lm \ (C \ T_s s^2 R + s \ T_s + 2)}
\]  
(2.62)
Simplified forms of the $G_{od}$ functions for the flyback converter are shown in Table 2.1. The $z$ indexes are for the function's zeros, and $p$ indexes are for the function's poles. The ideal case is when the esr of the output capacitor is not taken into account. The non ideal case is with the esr.

Table 2.1 Simplified control-to-output transfer functions for a flyback converter.

<table>
<thead>
<tr>
<th>Flyback</th>
<th>CCM Ideal</th>
<th>CCM Non Ideal</th>
<th>DCM Ideal</th>
<th>DCM Non Ideal</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{\bar{V}_o}{I_1}$</td>
<td>$K \cdot \frac{(s - s_{z_1})}{(s + s_{p_1})(s + s_{p_2})}$</td>
<td>$K \cdot \frac{(s - s_{z_1})(s + s_{z_2})}{(s + s_{p_1})(s + s_{p_2})}$</td>
<td>$\frac{K}{(s + s_{p_1})(s + s_{p_2})}$</td>
<td>$\frac{(s + s_{z_1})}{(s + s_{p_1})(s + s_{p_2})}$</td>
</tr>
</tbody>
</table>

It can be seen that presence of the esr in the model complements the transfer function with an additional zero.

An example Bode plot for CCM can be seen in Fig.2.19 [F7]. In Fig.2.19 the solid line represents the case when esr is present, and the dashed line without the esr.

![Bode Diagrams](image)

Fig. 2.19: Flyback converter in CCM, an ideal (dashed line) and non-ideal (solid line) cases.

The gain response, Fig.2.19, is typical for a second order system, but the slope changes from -40dB/dec to 0dB/dec due to the two zeros of the transfer function. In the phase diagram, Fig.2.19, the first zero is caused by the esr and the second is a right half plane zero (RHP) determined by the load resistance and the effective value of the magnetising...
inductance. For the ideal conditions, the effect of the right half zero is still present, but the effect of the zero introduced by the \( \text{esr} \) has disappeared.

In DCM the non-ideal and the ideal case are shown in Fig. 2.20. There is no RHP's effect. Only the effect of the zero introduced by the \( \text{esr} \) is present, boosting the phase to \(-90^\circ\), as expected. In the ideal case, the effect of the parasitic element is not present, so the response is like an ideal second order system.

![Bode Diagrams](image)

Fig. 2.20: Flyback converter in DCM, an ideal (dashed line) and non-ideal (solid line) cases.

2.2 Forward converter

The forward converter is shown in Fig. 2.21. This transformer-isolated converter is based on the buck converter [G1]. It requires a single transistor, and hence finds application at power levels lower than those commonly encountered in the full-bridge and half-bridge configurations. Its less pulsating output current (when compared with flyback topology), makes the forward converter well suited for applications involving high output currents. The maximum transistor duty cycle is limited; for the common choice \( N_1 = N_2 \), then the duty cycle is limited to the range \( 0 \leq D \leq 0.5 \).
Fig. 2.21: Single-switch forward converter.

In this topology the transformer ideally transfers the energy from the primary to the secondary side without storing any energy, but due to the non-ideal characteristic of the windings, a small magnetizing inductance is present. Some energy is stored in the core, and an additional winding, $N_2$, must be added to provide a path to the magnetizing energy to be discharged, $D_1$, to avoid transformer saturation. The transformer magnetising current, $i_{lm}$, is reset to zero while the transistor is in the off-state. The magnetising inductance, $L_m$, in conjunction with diode $D_1$, must operate in the discontinuous conduction mode, [G1] [G2]. The output inductor, $L$, in conjunction with diode $D_3$, may operate in either continuous or discontinuous conduction mode. In this case the magnetising inductance of the transformer and the parasitic elements in the inductor and the capacitor must be taken into account during modelling [F7].

In continuous conduction mode three time intervals are taken into consideration [G1]. The first time interval corresponds to the time that the transistor is on. The second and the third time intervals correspond to the off-time. The second time interval begins when the transistor is switched off and its duration is proportional to $D_1$ and $N_2/N_1$. When the magnetising current reaches zero, time interval three starts, and finishes when the transistor is switched on again.

Simplified form of $G_{od}$ functions for forward converters in CCM and DCM are shown in Table 2.2. The $z$ indexes are for the function’s zeros, and $p$ indexes are for the
function's poles. The ideal case is when the $esr_L$ and the $esr_C$ are not taken into account. In non-ideal case the $esr_C$ only is included.

Table 2.2 Simplified control-to-output transfer functions for a forward converter.

<table>
<thead>
<tr>
<th>Forward</th>
<th>CCM Ideal</th>
<th>CCM Non Ideal</th>
<th>DCM Ideal</th>
<th>DCM Non Ideal</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{\bar{v}_o}{\bar{a}_i}$</td>
<td>$K\frac{(s+s_p)}{(s+s_p)(s+s_p_1)}$</td>
<td>$K\frac{(s+s_p)}{(s+s_p)(s+s_p_1)}$</td>
<td>$K\frac{(s+s_p)}{(s+s_p_1)}$</td>
<td>$K\frac{(s+s_p)}{(s+s_p_1)}$</td>
</tr>
</tbody>
</table>

The Bode diagram of the system for the non-ideal and the ideal case is shown in Fig. 2.22. In the non-ideal case the gain falls with a slope of -40dB/dec, until the zero introduced by the $esr$ of the capacitor changes it to -20dB/dec. This effect can be observed in the phase diagram, as well, on the change of phase from -180°, due to the two poles, to -90°, see Table 2.2. It was observed that there was little variation on the response of the circuit when the resistive losses in the inductor were eliminated from the circuit. And so in practice can be eliminated from the model. For the ideal case, shown in the same figure, the effect of the zero is removed by removing the parasitic elements, so the system behaves as an ideal second order system.

![Bode Diagrams](image)

Fig. 2.22: Forward converter in CCM, an ideal (dashed line) and non-ideal (solid line) cases.
In DCM, a fourth interval is considered, when both, the inductor and magnetising currents are equal to zero [G1], [G2]. The high frequency pole due to the dynamics of the inductor is not included in the model, it has a negligible effect over the low frequency converter dynamics. The non-ideal and the ideal conditions response are plotted in Fig.2.23, for the non-ideal case, the response is a first order system, with pole due to the capacitor and a zero due to the $esr_C$. In the ideal case, the effect of the $esr_C$ is removed and only the effect of the pole due to the capacitor is present.

![Bode Diagrams](image)

Fig. 2.23: Forward converter in DCM, an ideal (dashed line) and non-ideal (solid line) cases.

2.3 Half-bridge converter

The half-bridge transformer-isolated buck converter is shown in Fig.2.24. This circuit is similar to the full-bridge, [G1], [G3], where two transistors and their antiparallel diodes have been replaced by capacitors $C_1$ and $C_2$. The operation theory of the converter can be found in many books [G1], [G2], [G3]. Here we concentrate on the practical aspects of this topology. This configuration needs only two transistors, but they must handle larger currents when compared with the full-bridge.
Fig. 2.24: Half-bridge transformer-isolated converter.

As a consequence, the half-bridge configuration finds application at lower power levels (usually below 750W), for which transistors with sufficient current rating are readily available. The utilisation of the transformer core is good. The transformer magnetising current can be both positive and negative, hence the entire core B-H loop can be used. The transformers primary winding is effectively utilised. But the centre-tapped secondary winding is not, since each half of the centre-tapped winding transmits power only during alternate switching periods.

Because of the complete B-H loop use, this converter can be modelled as two separated circuits (half circuit phenomena), each circuit is modelled depending upon which transistor is on. Some energy is stored in the magnetising inductance, but because the primary is driven in both directions, natural reset is applied avoiding possible transformer saturation. The magnetising inductance of the transformer, the $esr_L$ of the inductor and the $esr_C$ of the capacitor were modelled.

In continuous conduction mode four time intervals are taken into consideration, but the third and the fourth time intervals must be equal to the first and second time intervals, so the analysis can be reduced to the first two, extending our results to the full model, Fig.2.25a.
Fig. 2.25: Half-bridge converter waveforms: a) CCM, b) DCM

The response of the half-bridge converter with parasitic elements and without them is plotted in Fig.2.26. In the non-ideal case, the effect of the zero introduced by the $esr$ can be seen on the change, from $-40\text{dB/dec}$ to $-20\text{dB/dec}$, in the slope of the gain magnitude and the boost from $-180^\circ$ towards $-90^\circ$ in the phase response. The simplified forms of $G_{od}$ for an ideal and non-ideal cases can be seen in Table 2.3.

Table 2.3 Simplified control-to-output transfer functions for a half-bridge converter.

<table>
<thead>
<tr>
<th>Half-bridge</th>
<th>CCM Ideal</th>
<th>CCM Non Ideal</th>
<th>DCM Ideal</th>
<th>DCM Non Ideal</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{\bar{v}<em>{o}}{d</em>{1}}$</td>
<td>$K \cdot \frac{(s + s_{1})}{(s + s_{p_{1}})(s + s_{p_{2}})}$</td>
<td>$K \cdot \frac{(s + s_{1})}{(s + s_{p_{1}})(s + s_{p_{2}})}$</td>
<td>$\frac{K}{(s + s_{p})}$</td>
<td>$\frac{K}{(s + s_{p_{1}})}$</td>
</tr>
</tbody>
</table>
In DCM the loss-free resistor model \([G_1]\) was applied and a third time interval is considered when the output inductor current is zero and the magnetising current remains constant until the second transistor is turned on and the current change of direction. As in the CCM case, the circuit can be analysed taking only the three first time intervals, Fig.2.25b. The non-ideal system and the ideal response are plotted in Fig.2.27, the non-ideal case is a first order system response, with a pole due to the capacitor and a zero due to the \(esr\). In the ideal case, when the effect of the \(esr\) is removed, the pole due to the capacitor is present only. Simplified form of \(G_{od}\) for an ideal and non-ideal cases in DCM can be seen in Table 2.3.

Fig. 2.26: Half-bridge in CCM, an ideal (dashed line) and non-ideal (solid line) cases.

Fig. 2.27: Half-bridge in DCM, an ideal (dashed line) and non-ideal (solid line) cases.
Chapter 3

Flyback Converter Switch Waveforms Analysis

This chapter gives a theoretical justification to extracting the output voltage from the switch voltage. The oscillations that are recorded on the input voltage, the switch voltage and the output voltage are studied in detail, using a parasitic model of the converter. Filtering of high frequency components is investigated. Finally an experimental validation of the output voltage extraction technique is extensively undertaken, under various load and line conditions. It is proven by both analysis and recorded results that the oscillation on the input are generally speaking decoupled from those recorded on the output.

3.1 Switch Voltage of the Flyback Converter

The proposed control methodology is based on the fact that the information about the output voltage is available from the primary switch voltage, $v_{sw}$, during the off-time, Eq.3.1.

$$v_{sw} = v_{in} + (v_o + v_F) \cdot \frac{N_p}{N_S} \quad (3.1)$$

Where: $v_{in}$ is the input voltage, $v_o$ is the output voltage, $v_F$ is the forward voltage drop of the output diode, $N_p/N_S$ is the turn ratio of the flyback transformer. To perform more detailed analysis of Eq.3.1 we introduce AC perturbations:

$$v_{sw} = V_{sw} + \tilde{v}_{sw} \quad (3.2)$$

$$v_{in} = V_{in} + \tilde{v}_{in} \quad (3.3)$$

$$v_o = V_o + \tilde{v}_o \quad (3.4)$$

$$v_F = V_F + \tilde{v}_F \quad (3.5)$$

The widely known DC part of Eq.3.1 to Eq.3.5 is [G9]:

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Equation with AC terms based on Eq.3.1 to Eq.3.5 is:

\[ V_{sw} = V_{in} + (V_o + V_F) \cdot \frac{N_p}{N_S} \]  \hspace{1cm} (3.6)

Eq.3.7 can be simplified by neglecting \( v_F \), Eq.3.8. The assumption is that \( v_F = 0 \), is valid assuming that the forward recovery time of the output diode and the associated high frequency oscillations \([G6]\) ring out within the time delay of the control circuit. This assumption is made following tests conducted on the prototype; see Fig.3.8c, Fig.A2.3.12c, Fig.A2.3.19c and Fig.A2.3.23c. Here we want to emphasise that \( v_F \) is not the forward voltage drop change due to the changing current (according to \( v_F = f(i_F) \)), but an AC perturbation on top of \( V_F \) due to the forward recovery of the device and circuit parasitics. And \( V_F \) is dictated by \( v_F = f(i_F) \). This time is relatively constant for the same diode type (around 100ns for dual Schottky diode ST6100) and is smaller than the control circuit time delay (around 500ns) discussed later in Chapter 10. After the 100ns \( v_F \) follows a characteristic \( v_F = f(i_F) \) \([ST\ data\ sheet]\).

\[ \tilde{V}_{sw} = \tilde{V}_{in} + (\tilde{V}_o + \tilde{V}_F) \cdot \frac{N_p}{N_S} \]  \hspace{1cm} (3.8)

Eq.3.8 represents the AC oscillations of the switch on the top on DC level represented by Eq.3.6.

The output voltage calculated on the primary side during the off-time from Eq.3.1 can be expressed:

\[ v_{oc} = (v_{sw} - v_m) \cdot \frac{N_S}{N_p} - v_F \]  \hspace{1cm} (3.9)

Combining this equation with Eq.3.2 to Eq.3.5 \((v_F = 0)\) with Eq.3.8 we obtain:
Now using the output voltage expression derived from Eq.3.6 and substituting it into Eq.3.10, it can be written as:

\[ v_{oc} = (V_{sw} - V_m) \cdot \frac{N_S}{N_P} - V_c + \tilde{v}_o \]  

(3.10)

\[ v_{oc} = V_o + \tilde{v}_o \]  

(3.11)

\[ v_{oc} = v_o \]  

(3.12)

Eq.3.12 shows that for an ideal transformer, we obtain the exact output voltage on the primary side of the converter during the off-time. The input voltage ripple is rejected in subtraction process. A number of practical measurements under different circuit conditions are presented later to demonstrate that the \( \tilde{v}_{sw} \) contains \( \tilde{v}_o \) and \( \tilde{v}_m \), and that the \( \tilde{v}_m \) is rejected in the subtracting process, Eq.3.10.

3.2 Analysis of parasitic effects on the switch voltage

The output voltage curve is more complex than that calculated in Chapter 2. The input voltage is also far from an ideal DC level. The nonlinearity of these two signals has an impact on the switch voltage. Below we present and analyse the oscillations on top of the \( v_{sw} \) signal, together with the interdependence between the primary and secondary waveforms. This material can be used for further extended analysis. The circuit is configured as an isolated topology but in order to observe the primary and secondary waveforms simultaneously, using an oscilloscope, the primary and secondary grounds are shorted together.
Fig. 3.1: Test points of a flyback converter circuit, the isolation barrier broken during the measurement.

Paragraph § 3.2.1 shows details of selection of $C_{pd}$ and $R_{pd}$ – damping network. § 3.2.2 presents analysis of the resonant circuit in DCM. The experimental results are in § 3.3. The experiments in section 3.3 show the waveforms of $v_{in}$ and $v_o$ plus their effect on the switch voltage, $v_{sw}$. These experiments change the values of $C_{in}$, $C_o$ and $I_o$ to observe the effect on $i_{sw}$, $v_{sw}$, $v_{in}$, $v_o$ and in some cases $v_F$, see Table 3.1. The input voltage is, $V_{in}=18V$ and the output voltage is, $V_o=3.3V$. The converter was operating in DCM – the worst case.

Table 3.1 Experiments for $V_{in}=18V$ and $V_o=3V3$, DCM

<table>
<thead>
<tr>
<th>Exp. No.</th>
<th>$C_{in}$ [$\mu$F]</th>
<th>$C_o$ [$\mu$F]</th>
<th>$I_o$ [A]</th>
<th>$V_F$</th>
<th>Paragraph</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>10+100</td>
<td>0.62</td>
<td>Yes</td>
<td>3.3.1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>10+6800</td>
<td>0.62</td>
<td>Yes</td>
<td>3.3.2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>10+2*6800</td>
<td>0.62</td>
<td>No</td>
<td>3.3.3</td>
</tr>
<tr>
<td>4</td>
<td>1+820</td>
<td>10+100</td>
<td>0.62</td>
<td>Yes</td>
<td>3.3.4</td>
</tr>
<tr>
<td>5</td>
<td>1+820</td>
<td>10+6800</td>
<td>0.62</td>
<td>Yes</td>
<td>3.3.5</td>
</tr>
<tr>
<td>6</td>
<td>1+820</td>
<td>10+2*6800</td>
<td>0.62</td>
<td>No</td>
<td>3.3.6</td>
</tr>
<tr>
<td>7</td>
<td>1+820</td>
<td>10+100</td>
<td>0.4</td>
<td>No</td>
<td>3.3.7</td>
</tr>
</tbody>
</table>
3.2.1 Practical implementation of main switch damping network

The circuit in Fig.3.1 contains a damping network \(C_{pd}\) and \(R_{pd}\) [G5]. A response without damping is shown in Fig.3.2. In order to calculate \(C_{pd}\) and \(R_{pd}\) [G5],[G7] we first read the ringing frequency, \(f_i=14.28\,\text{MHz}\), from Fig.3.2b.

Next we add a capacitor \((C_{pd}=370\,\text{pF})\) across the primary winding of the flyback transformer and again read the ringing frequency. The capacitance (damping capacitance \(C_{pd}\)) is chosen to half the ringing frequency, [G7]. Having this information the resistor value can be calculated using the basic resonant frequency equations as follow [G5].

\[
\begin{align*}
f_i &= \frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} \quad \text{(Eq.3.13)} \\
\frac{1}{2} \cdot f_i &= \frac{1}{2\cdot\pi\cdot\sqrt{L\cdot (C + C_{pd})}} \quad \text{(Eq.3.14)} \\
C &= \left(\frac{f_1}{\frac{1}{2} \cdot f_i}\right)^2 = \frac{C_{pd}}{3} \quad \text{(Eq.3.15)} \\
L &= \frac{1}{4\cdot\pi^2 \cdot f_i^2 \cdot C} \quad \text{(Eq.3.16)} \\
R_{pd} &= \sqrt{\frac{L}{C}} \quad \text{(Eq.3.17)}
\end{align*}
\]

In our case \(R_{pd}=95.2\,\Omega\), so \(R_{pd}=91\,\Omega\) – the closest available value.
3.2.2 Resonant network in DCM

When the converter is in DCM then the current oscillates with frequency dictated by the magnetising inductance of the transformer, $L_m$, and a capacitance $C_{eq}$, Eq.3.18 [G7],

$$C_{eq} = C_{DS} + C_{pd} + C_{p-tr} + C_{Dj} \cdot \left(\frac{N_2}{N_1}\right)^2 + C_{par}$$ (3.18)

Where: $C_{DS}$ - Drain-to-Source capacitance, $C_{pd}$ - a damping capacitance across the switch [G4], $C_{p-tr}$ - flyback transformer primary winding capacitance, $C_{Dj}$ - junction capacitance of the output diode, $C_{par}$ - a parasitic capacitance. The parasitic capacitance, $C_{par}$ can be estimated once we have DCM oscillation frequency and $C_{p-tr}$. The $C_{p-tr}$ can be measured. In our case it was measured using a Gain and Phase analyser (HP4194A), the equipment was also used to calculate equivalent circuit’s components values. The measurement was done with secondary side disconnected, Fig.3.4a. The same measurement was done for the secondary side, Fig.3.4b. Capacitance between the
primary and the secondary winding was measured too, Fig.3.4c. The equivalent circuit for the current oscillations in DCM is shown in Fig.3.3. The resonant frequency in circuit from Fig.3.3 can be calculated from the equivalent admittance, Eq3.19.

\[
Y_{eq} := \frac{1}{R_{p\_tr} + I \omega L_m} + \frac{1}{R_{is} - \frac{I}{\omega C_{DS}}} + I \omega C_{sum} + \frac{1}{R_{pd} - \frac{I}{\omega C_{pd}}}
\]  

(3.19)

Where:

\[
C_{sum} := CD_{jp} + C_{par} + C_{p\_tr}
\]

(3.20)

Hence the resonant frequency can be calculated, but because of the complexity and size of the equation we decided not to show it here, see attached floppy disk. Once we have measured that frequency, \(f = f_{resDCM}\), the value of \(C_{sum}\) can be calculated, Eq.A1.3.21.

Next \(C_{par}\) can be calculated from Eq.3.20. In our case \(C_{par} = 54.06\text{pF}\). This calculation is an example of complexity of "a simple" industrial flyback converter. Usually in literature we deal with simplified analysis [A14].

Fig. 3.3: Parallel resonant circuit during DCM.
3.3 Experimental results

In this paragraph results from the first experiment can be seen. The rest of the results with comments can be seen in Appendix 2.

For chosen input voltage $V_i=18\text{V}$ and $V_o=3.3\text{V}$ values of the output and the input capacitors were changed. Tests were done for the output currents $I_o=0.62\text{A}$ and $I_o=0.4\text{A}$. The converter was operating in DCM – the worst case test conditions.
Experiment 1

Fig.3.5, Fig.3.6 and Fig.3.8 are for $I_o=0.62A$ The input capacitance is $C_{in}=1\mu F$ and the output capacitance is $C_o=10\mu F$ ceramic cap. plus $100\mu F$ tantalum cap. In Fig.3.5 can be seen the input voltage, $v_{in}$, and the output voltage, $v_o$. It can be seen that there is no correlation between amplitudes of these signals. The shapes are also different.

Fig. 3.5: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F$, $C_o=10\mu F+100\mu F$: a) $v_{in}$, b) $v_o$.

Fig. 3.6: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F$, $C_o=10\mu F+100\mu F$: a) $v_{2w}$, b) zoom of $v_{2w}$.
In Fig. 3.6 can be seen the switch voltage, $v_{sw}$, during the off-time. In Fig. 3.6b can be seen the zoom of $v_{sw}$. The main shape of this signal is difficult to describe in details but it can be seen that it is formed by summary of $v_{in}$ and by $v_o$ - respectively in Eq. 3.1.

In Fig. 3.7 can be seen current waveform, $i_{sw}$, flowing through the resistor $R_{is}=1.7\Omega$, see Fig. 3.1. It was measured as a voltage across the resistor, so $i_{sw}=v_{Ris}/R_{is}$. The complete waveform is shown in Fig. 3.7a. The zoom of the current during the off-time is shown in Fig. 3.7b. This is a current flowing in the opposite direction through the capacitance of the MOSFET $Q_1$, $C_{DS}$. This current is approaching equal to zero level with a long time constant. The initial ripple frequency, Fig. 3.7c, is dictated by forward recovery time of the output diode.

**Fig. 3.7:** $V_{in}=18\text{V}$, $V_o=3.3\text{V}$, $I_o=0.62\text{A}$, $C_{in}=1\mu\text{F}$, $C_o=10\mu\text{F}+100\mu\text{F}$: a) $i_{sw}$ complete, b) zoom of $i_{sw}$ around zero level, c) zoom of $i_{sw}$ at the beginning of the off-time.
The forward voltage drop of the output diode can be seen in Fig.3.8. The complete waveform is shown in Fig.3.8a. The forward recovery behaviour can be seen in Fig.3.8c. When it is compared with Fig.3.7c it can be seen that the peak values appear at the same time. Transient oscillations are finished after 100ns. The zoom of complete slope can be seen in Fig.3.8b. After the initial oscillations $v_F$ follows $v_F=f(i_F)$ curve, as per the catalogue.

![Waveform diagrams](image)

Fig. 3.8: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F$, $C_o=10\mu F+100\mu F$: a) $v_F$ of the output diode - complete, b) zoom of the slope of $v_F$, c) zoom of the beginning of $v_F$. 

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3.4 Summary of the experiment

Due to comparative analyse of the presented results, Appendix 2, can be said that change of the output capacitance mainly changes the output voltage waveform. It has no obvious impact on the input voltage oscillations. And vice versa the change in the input capacitance mainly changes the input voltage waveform. It has no obvious impact on the output voltage oscillations. Correctness of Eq.3.10 to Eq.3.12 is based on this assumption.

An equivalent circuit for the primary and the secondary sides, during the off-time, can be seen in Fig.3.28. This equivalent circuit is derived from comparative studies of experimental results from section 3.3, Appendix 2.

Fig. 3.28: An equivalent circuit for the primary and the secondary side oscillations analysis.
Chapter 4
Proposed Control Strategy

In many cases galvanic isolation between the input and the output of switch mode power supplies is desired. The basic idea of this research was derived from limitations of the commonly used isolation schemes.

In this chapter we review the existing isolation techniques and discuss their advantages and disadvantages.

As a consequence of this study then we present novel solutions to eliminate limitations of the existing techniques and to significantly improve performance.

4.1 Existing techniques

A challenge of providing galvanic isolation is not so much in the power stage as in the feedback path. The power path is naturally isolated by a transformer, which is routinely constructed with sufficient insulating material between the windings to meet the safety standards and the feedback path in a basic power converter can be isolated in four major places, Fig.4.1.

![Diagram of major isolation points in power converters](image-url)

Fig. 4.1: Major isolation points in power converters.
Before we start our discussion about the major isolation points, it must be said that additional the path where isolation may be required is the bias power for the signal processing blocks that must be powered-up before the switch mode power supply can be operated. If any of these blocks happen to be on the secondary side, this bias power must be provided with the same safety isolation as the output of the converter [E1].

In the control path, the designer may choose the following options [G4], [E1]:

- **Isolation of the output information.** It can be done with a secondary driven amplitude modulator, which transmits the DC output voltage across an isolating pulse transformer to the primary side. It is a relatively complex method for isolating the measurement of the output voltage and adds extra components to the circuit – a switch, transformer with the reset winding, two diodes, averaging capacitor and resistor.

- **Isolation of the analogue error signal.** This is the most popular and widely used technique for isolation – placing the barrier between the analogue and digital portions of the feedback path. Main isolation techniques in this case are:
  - **Opto-couplers** – there is a problem with CTR degradation over time and temperature, § 1.1.
  - **Transformers** – the problem is that the control signal must include DC information to hold the power supply’s output constant. To get DC through a transformer requires some form of carrier modulation. The required circuitry normally is complex enough to preclude this approach for most applications.
  - **Capacitors** (not popular) – they must be high voltage types (to meet the standards) and there is at least two required. They are not a very cost effective solution.

- **Isolation of the digital signal path.** Only digital information crosses the isolation boundary. This can be done with either opto-coupler or a transformer. Advantage of this approach is low susceptibility to noise transients, but complexity of the circuit is a serious disadvantage.

- **Isolation of the digital power path.** In this case transformers are usually applied between the PWM/PFM output drivers and the main power switches. This approach
puts all the control on the secondary side of a converter. With close DC coupling to the outputs, high accuracy and good protection can readily be provided. But there are two problems with this method: 1) The isolating transformers must also provide drive power to the switches and 2) the secondary side control needs an isolated power source.

It looks as each of the mentioned isolation techniques have some disadvantages. An alternative solution to these problems is a system without an overall control loop [G4], there is no feedback path. In this situation there is feed-forward or current-mode control on the primary and separated regulators on the secondary, this solution gives excellent results. The primary side circuits can be supplied from the line voltage and the secondary circuits need low-voltage auxiliary winding from the power transformer. This complicates the transformer manufacturing process.

A better solution would be a system with primary side control only, without direct output voltage sensing. Known solutions to this are miscellaneous techniques with an averaging capacitor on the primary side, fed through a diode from the auxiliary winding on the power transformer [G4]. In the case of the flyback transformers it is even easier, there is no need for an additional winding – voltage across the switch in its off-state is used. But this method has the disadvantage that it is an average mode control. The dynamic performance is not good and additionally the control accuracy strongly depends on the converter operation mode.

Obviously the best solution of the above mentioned problems would be some sophisticated and simple control circuit placed on the primary side and based only on signals available there. Without any averaging components, responding instantly within the present operation cycle (or the latest in the next cycle) to the line and the load changes, additionally suitable to integrate into one IC. This is the basic challenge, which was undertaken in this thesis.

4.2 Basic idea of proposed solution

To test the control mechanism we have decided to maintain constant off-time and vary the on-time, Fig.4.2a, this means it is pulse frequency modulation (PFM). It is
the most interesting to us case and is good enough to check the control mechanism. This control solution can also be applied to: variable off-time and constant on-time, Fig.4.2b, variable off-time and variable on-time, Fig.4.2c, ad constant frequency flyback converters, Fig.4.2d.

Fig. 4.2: Possible modulations implementations with proposed control technique.

All the control signals are calculated on the primary side of the converter, Fig.4.3, providing the same full galvanic isolation between \( V_{in} \) and \( V_o \).

Fig. 4.3: Basic diagram of the primary side controlled flyback converter.

According to Eq.3.6, in an ideal case, during CCM in steady state operation \( V_{sw} \) should be at a constant level during the off-time. In reality the voltage decays due to the output diode characteristic, imperfection of the transformer and the output capacitor nature (esr, esl and structure) see Fig.4.4. All these parts are secondary current sensitive.
In addition these voltage drops are "amplified" by the flyback inductor turns ratio before they appear on the primary side.

Because of the above-mentioned problems the best place to apply Eq.3.6 is near the beginning of the off-time when the switch voltage reaches its highest point (Detection area, Fig.4.4), neglecting an initial transients. This requires the circuit to store the initial value of a signal for the rest of the off-time, see Fig.4.5, as it would be calculated from an ideal switch voltage in CCM. To meet such a demand we have decided to detect and store the desired value using a peak detector (see chapter 5). Reset of the peak detector takes place in each on-time. In summary we have obtained a novel solution for the output voltage sensing in the flyback converter. The proposed solution is independent of the secondary side circuit features and what is the most important is the converter operation mode independent too, Fig.4.5. The output voltage is checked in each cycle during the off-time, this allows correcting it in every cycle providing cycle by cycle control of the isolated flyback converter. In this case when the peak detector is used, inter-cycle (inter-off-time) changes of the output voltage can be sensed only in one direction, Fig.4.6, when the voltage rises. Decreased voltage will only be sensed in the next cycle, this feature can be a disadvantage of the proposed solution.

Fig. 4.4: Voltage across the primary switch, Q₁, CCM.
Fig. 4.5: Novel solution visualisation: a) CCM, b) DCM.

Fig. 4.6: Inter-cycle $V_o$ changes detection: a) step-up load, b) step-down load.
The proposed solution may be implemented by means of two major control mechanisms.

(1) General implementation, where either the on-time or the off-time or both may be variable or constant, Fig. 4.7.

(2) Special implementation where the on-time varies and is calculated during the constant off-time, Fig. 4.8.

In the second case the method of calculation limits the maximum on-time to be shorter than the off-time, but this limitation may be overcome by the method shown in § 6.1 and § 6.2.

Fig. 4.7: Time waveforms for variable off-time control scheme.

In this work we have concentrated mainly on the second solution, with the restricted on-time. It is a relatively more complex solution but the results obtained from the prototype give us strong background for theoretical verification of the other possible topologies, (see chapter 6), with this novel control mechanism.

Fig. 4.8: Time waveforms for constant off-time control scheme.
Additionally, in the case of calculating the on-time, $t_{on(k+1)}$, within the off-time, $t_{off(k)}$, we have avoided a problem with the reset time of the peak detector, discussed in § 6.1 and § 6.2 control schemes.

As we said the calculation takes place during the off-state of the converter, called, $t_{off}$. A control signal for the MOSFET in next cycle, $(k+1)$, (on-state, $t_{on(k+1)}$) is calculated during each $t_{off(k)}$ of the converter, see Fig.4.8. By comparing the slope of a function generator SG1, with the peak detector output signal, PD1, we determine a time that can be used for control in the next cycle. See Fig.4.9. Notice that the "Calculated on-time" is between a cross-over time, $t_c$, and the end of the off-time. Due to this the "Calculated on-time" can be easily reflected into the next cycle as $t_{on(k+1)}$. It is done using two slopes, SG2 and SG3, and a comparator, see § 5.4.

Fig. 4.9: On-time calculation mechanism within off-time.

The forward voltage drop of the output diode, $V_F$, is assumed as a constant value. This degrades accuracy of the regulation but has no effect on the control mechanism. The background of this assumption is explained in § 5.5. By using a synchronous rectifier the accuracy can be improved, see § 5.6.
Chapter 5
The Control Implementation

In this chapter details of the complete converter and controller are discussed. Aspects of the control circuit such as the control error signal, the first trial value of the error gain and offset voltage and the calculated on-time reflection with overcurrent protection are discussed.

The start-up circuit is explained in details, showing how it achieves the fastest ramp up of the output voltage possible, yet not over stressing the components, after ramping the circuit switches to normal mode.

Discussion about the output diode and an alternative solution with a synchronous rectifier is also undertaken.

5.1 The control circuit description

The following description of the control circuit operation is referred to Fig.5.2. The control circuit has three input pins and one output, see Fig.4.3 and Fig.5.2. The following signals are required: the input voltage, $V_{in}$, the switch voltage, $V_{sw}$ and the voltage across the current sensing resistor, $R_{IS}$ ($V_{IS}$). The output signal of the control circuit is the control signal of the MOSFET $V_{GS}$.

An important aspect is that a regulation error, $V_E$, is calculated in the opposite way, Eq.5.1, to the commonly used method, Eq.5.2. This is dictated by the control methodology.

$$V_E = V_o - V_{ref}$$

$$V_{E\text{traditional}} = V_{ref} - V_o$$

According to Eq.5.1, the regulation error signal, $V_E$, Eq.5.3 (DC large signal equation), is calculated due to the output voltage, $V_o$, from Eq.3.10 and the reference voltage, $V_{ref}$. This takes place in each off-state of the converter operation and is done by using wide bandwidth electronic components, see Chapter 7.

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From Eq.5.3 (see block diagram Fig.5.2) it can be seen that the first step is to subtract input voltage, $V_{in}$ from the switch voltage, $V_{sw}$. During the on-time this signal must be limited, $V_{sw}-V_{in}>0$, to stay within the common mode signal range of the components. The limitation is provided by a signal limit, $SL$. The signal obtained is amplified, $K_I$. The gain, $K_I$, is equal to $N_I/N_P$ and is less than 1. Subtracting from this signal the forward voltage drop of the output diode, $V_F$, the output voltage $V_{oc}$ is obtained. This signal is used to calculate $V_E$ and also provides information about the converter output in the start-up circuit. $V_E$, is multiplied by an absolute value of the error, $|V_E|$, and gives the square error with preserved sign, $+/-V_E^2$, see Eq.5.4 and Fig.5.1.

$$\frac{+/-V_E^2}{+/-V_E^2} = V_E * |V_E|$$

The square error is amplified by $K_2$. The first trial value for the gain is calculated according to the nominal offset voltage, $V_{offsetn}$, § 5.3, the maximum allowed error voltage, $+/-V_{Emax}^2$ and the common mode input voltage range of a comparator, $V_{comp}$ ($C_3$), see Eq.5.5. The final value of the gain is set experimentally as

$$K_2 = \frac{V_{comp} - V_{offsetn}}{+/-V_{Emax}^2}$$

The amplified error signal is shifted up by an offset voltage, $V_{offset}$ and fed to a peak detector, *Peak detector*, where the peak value is measured and held until the reset. The reset signal in this case is the on-time.
The output signal of the peak detector is fed to the negative input of a comparator, $C_3$, where it is compared with a slope, $SG_1$, (see Fig.4.9). The slope starts from zero level (after a reset during the on-time) and rises up to the maximum allowed level, $SG_{1\text{ max}}$, at the end of the off-time. The slope can be described by a mathematical equation, Eq.5.6.

$$SG_1 = \tan(\alpha_{SG_1}) \times t$$ \hspace{1cm} (5.6)

Where:

$$\tan(\alpha_{SG_1}) = \frac{SG_{1\text{ max}}}{t_{\text{off}}}$$ \hspace{1cm} (5.7)

The output signal of the comparator, $C_3$, is calculated during the off-time and is reflected into the next operation cycle as the on-time. This is done with two slopes $SG_2$, $SG_3$ and a comparator, $C_4$, (see Fig.4.9 and § 5.4). The slope $SG_2$ starts at the cross-over time, $t_c$. The $\tan(\alpha_{SG_2})$ is the same as $\tan(\alpha_{SG_1})$. The slope $SG_3$ starts at the end of the off-time and rises up twice faster than $SG_2$, Eq.5.8 due to this, the crossing point of the slopes sets the end of the on-time. The reset of the slopes starts at the beginning of the off-time.

$$SG_3 = \tan(\alpha_{SG_3}) \times t = \tan(2 \times \alpha_{SG_2}) \times t$$ \hspace{1cm} (5.8)
Fig. 5.2: Block diagram of the control circuit, together with the start-up circuit.
The output signal of the comparator $C_4$ is fed to the logic AND gate, *Logic1*, where it is verified with two other signals, see Fig.5.3 and Fig.5.4. One of them is "low" during the off-time, *Logic2 output*, this avoids turning on the primary switch during the off-time. The other one comes from the over current protection circuit, comparator $C_I$. When the primary side current, $I_P$, is below the limit, $I_{PL}$, then the output of $C_I$ stays at logic level "high". The on-time is controlled by the output of $C_4$, see Fig.5.3. If $I_P$ exceeds the limit, then the output of $C_I$ goes "low". The transition from "high" to "low" triggers constant off-time. Slopes $SG2$ and $SG3$ are reset before they cross each other. The on-time is limited by the current limit circuit, see Fig.5.4.

![Diagram](image)

Fig. 5.3: Signals verification at logic AND gate, *Logic1*, the primary side current, $I_P$, below a current limit, $I_{LP}$.

The output signal of the AND gate, *Logic1*, resets directly the peak detector. The same signal is fed to the MOSFET’s driver and to a constant off-time generator, *Constant off-time (2)*, through the start-up circuit, *Test start-up circuit*. The start-up
The circuit is described in details in § 5.2. The constant off-time is triggered by the decaying output signal of the AND gate.

![Diagram of signals verification at logic AND gate](image)

**Fig. 5.4**: Signals verification at logic AND gate, *Logic1*, the primary side current, *I_p*, exceeds the current limit, *I_{LP}*.  

In the proposed control circuit the on-time changes according to the regulation error and the offset voltage, *V_{offset}*. The on-time gets longer when the regulation error is negative and vice versa. The on-time is also inverse proportional to the offset voltage – this provides line regulation, § 5.3. As a result the output voltage of the flyback converter is maintained at the desired level, this is, variable frequency, cycle by cycle output voltage mode control. The same circuit can operate at a heavy load in CCM and at light loads in DCM.
5.2 Start-up circuit

The proposed control solution requires a start-up circuit, which will power-up the converter and at a certain time switch itself to normal constant off-time control.

During the start-up the voltage feedback loop has no influence on the on-time. The on-time is controlled by a start-up circuit operating in current mode control. The converter is switched from current mode control to voltage mode control automatically at the end of the start-up process. The start-up circuit is designed to work with the proposed control mechanism. A block diagram of the circuit can be seen in Fig.5.5. The circuit operates with constant off-time and variable on-time. The on-time is controlled by a current limit ramp. The end of the start-up is when the output voltage sensed during the off-time is greater than a threshold voltage. Following detailed description of the circuit operation is referred to Fig.5.5, Fig.5.6 and Fig.5.7.

At the beginning of the powering-up process circuits $U_1$ and $U_2$ (74HC175 D Flip-Flop with Clock and Reset) are reset (active low) and initially set (high). This is done by simple $RC$ networks with AND gates. When $V_{cc}$ appears then after some time delay as set by $RC$ time constant the reset signal is finished, initial reset and the set signals appears, initial set. These signals are maintained at logic level high for the rest of the converter operation, this ensures that $U_1$ and $U_2$ change their output states only once at the end of the start-up process. The changes are triggered by the positive-going edge of the clock input, SET. Outputs $Q(U_1)$ and $Q(U_2)$ are initially low. In the prototype the reset of the whole system is manual however, it can be easily changed into an automatic process.

The constant off-time, Constant off-time(1), is generated by a retrigerable-resetable monostable multivibrator (HEF4528). The constant off-time is triggered by the negative-going edge. The inverting output is used, $\overline{Q}$ off-time (1). Constant off-time (2) is also shown as a part of the start-up circuit. The first positive going edge of Constant off-time (2) cuts off the start-up circuit and switches the converter into the voltage mode control. Constant off-time (1) can be different from Constant-off-time (2). This feature provides design flexibility e.g. Constant off-time (1) can vary: short at the early stage of the start-up process and longer later.

To switch between different signals some 3-State Noninverting Buffers, $TSB$ (74HC125), were used in the circuit too.
The primary side current is sensed with a current sensing resistor. The voltage from the current sensor, $V_{IS}$, is fed to the negative input, $C_{I-}$, of a comparator, $C_I$. The comparator compares $V_{IS}$ with a current limit ramp, current limit level and is fed to $C_{I+}$. When the primary side current, $I_p$, exceeds the current limit the on-time is ended and constant off-time starts, $\overline{Q}$ off-time (1). This signal goes through the input, $A_1$, of $TSB_i$ to the output, $Y_i$ and is fed to the MOSFET driver, $DR$. $OE_i$ is low because $V_o$ is calculated on the primary side, $C_{2+}$, during the off-time is below a threshold, output voltage threshold, $C_i$. 
Fig. 5.5: A block diagram of the start-up circuit.
Fig. 5.6: Signal waveforms of the start-up circuit.
The output of a comparator $C_2$, $C_2 \text{ out}$, is low. There was not a low-to-high transition of the clock input, $SET(U_1)$. The inverting output of $U_1$, $\bar{Q}(U_1)$, is high and so is $OE_2$ too. Therefore the output, $Y_2$, of $TSB_2$ is a high impedance output and this prevents a short-circuit between $Y_1$ and the control circuit through $TSB_2$. The same situation is in $U_2$. There was not a low-to-high transition at $SET(U_2)$. Constant off-time (2) is waiting for the first transition high-to-low of $\bar{Q}(U_1)$ through $TSB_3$. $OE_4$ is high so the output, $Y_4$, of $TSB_4$ is at high impedance. Due to the high impedance at $Y_4$ there is not a short-circuit between $Y_3$ and $Y_1=A_4$.

When the calculated primary side voltage exceeds output voltage threshold the output of $C_2$, $C_2 \text{ out}$, changes from low-to-high. This first transition changes outputs' states of $U_1$. The change high-to-low at $\bar{Q}(U_1)$ triggers the first pulse of Constant off-time (2), through $TSB_3$. This is the first time when the on-time is calculated in the control circuit. The reflected on-time will appear at $DR$ through $TSB_2$ - because now $OE_2$ is low. $Q(U_1)=OE_4$ goes high cutting off $\bar{Q}$ off-time (1).

A transition low-to-high at $Q$ off-time (2) $=SET(U2)$ changes outputs' states of $U_2$. Now, when $Q$ off-time (2) is triggered, $Q(U2)=OE_3$ is high – the output $Y_2$ is at high impedance. $\bar{Q}(U2)$ is low – $TSB_4$ is open. The voltage mode control loop is closed through $TSB_2$ and $TSB_4$. The control mode change takes place during Constant off-time (2) plus the remainder of Constant off-time (1), see on-time $t_{on}=A_4$, (more details later).

The start-up circuit has no influence on the on-time during normal operation of the converter and at this stage the comparator $C_1$ acts as an over-current detector. $C_2 \text{ out}$ is fed to an over-current protection circuit.

An important issue of the start-up circuit is the output voltage threshold, $C_2^-$. This voltage has to be less than the reference voltage, $V_{ref}$. To explain the reason lets
assume for a while that output voltage threshold=\(V_{\text{ref}}\). This means that the voltage mode control will be switched on when the output voltage of the converter is equal to \(V_{\text{ref}}\) and in this case we can consider two extreme examples: 1) when the sensed output voltage exceeds output voltage threshold at the very beginning of the off-time, see Fig. 5.8. 2) when the sensed output voltage exceeds output voltage threshold at the very end of the off-time, see Fig. 5.9. Additionally we assume that the converter operates in CCM at the end of powering-up, this means that the secondary current does not reach the zero level during the transient off-time. In both cases some overshoot appears so to avoid the overshoot it is necessary to set the threshold at least one overshoot amplitude below \(V_{\text{ref}}\). This requires calculation of the overshoot amplitude.

In the first case it can be seen that the transient off-time is equal to the normal off-time, Constant off-time (2), – neglecting time delays of electronic components. This is because Constant off-time (1) and Constant off-time (2) start at the same time. The voltage overshoot associated with this operation, can be calculated using known initial conditions.

\[
\text{output voltage threshold} = V_{\text{ref}}
\]

\[
\text{calculated output voltage}
\]

\[\overline{Q} \text{ off-time (1)}\]

\[Q \text{ off-time (2)}\]

\[\text{on-time } t_{\text{on}}\]

\[\text{transient off-time}\]

Fig. 5.8: The end of the powering-up process at the beginning of the off-time (1).
We know that the primary side current, \( i_{\text{in}} \), at the end of the former on-time, \( I_{\text{in(E)}} \), was equal to the current limit level, \( I_{\text{limit}} \). The initial condition, \( I_s(0) \), for the secondary side current, \( i_s \), can be found from Eq.2.15.

The output voltage, \( V_{\text{off}(0)} \), at the beginning of the transient off-time is equal to \( V_{\text{ref}} = \text{output voltage threshold} \), Eq.5.9.

\[
V_{\text{off}}(0) = V_{\text{ref}}
\]  

(5.9)

The voltage threshold, \( V_t \), can be calculated using Eq.5.10. Where \( V_{\text{off}} \) is from Eq.2.37.

\[
V_t = V_{\text{ref}} - V_{\text{off}}
\]  

(5.10)

In Eq.2.37 instead of \( V_{\text{off}}(0) \), \( V_{\text{off}(0)} \) is used which can be calculated combining basic equations from § 2.1.1.

In the second case the longest possible transient off-time appears. This is because \textit{Constant off-time (2)} starts at the end of \textit{Constant off-time (1)}. This does not increase associated overshoot, it even reduces the overshoot due to the smaller value of the secondary side current.
5.3 Offset voltage

In the ideal case when the output voltage is equal to $V_{ref}$ then $V_E$ is zero. In this case on-time will be calculated according to the offset, $V_{offset}$ and this means that $V_{offset}$ has to be a function of $V_{in}$, see Eq.5.11 - CCM and Eq.5.12 - DCM, Fig.5.13.

$$t_{on} = \frac{N_E}{N_S} \frac{V_o}{V_{in}} * t_{off}$$

(5.11)

$$t_{on} = \frac{V_o^2 \cdot L_m + \sqrt{L_m \cdot \left(V_o^2 \cdot L_m + 2 \cdot V_{in}^2 \cdot R \cdot t_{off}\right)}}{V_{in}^2 \cdot R}$$

(5.12)

Example of an on-time curve as a function of the input voltage, $V_{in}$, of a flyback converter is shown in Fig.5.10.

![On-time curve](image)

Fig. 5.10: Flyback converter $t_{on}=f(V_{in})$, $V_o=3.3V$, $f_s=100$ kHz, $t_{off}=5$ $\mu$s.

As it can be seen in Fig.5.10, this is not a linear function but this problem can be solved using fast analogue multipliers (e.g. MPY634), nevertheless we have decided to linearise the curve in a narrow range of the input signal and observe the behaviour of the
prototype. A possible future benefit from this approach is size and complexity reduction. This function can be realized using a voltage divider. For the input voltage range $V_{in}=16$ to $20V$ and nominal value $V_{nom}=18V$ linearisation gives good results, see Fig.5.11 (Maple geometry function). This means our offset voltage, $V_{offset}$, changes proportionally to $V_{in}$, see Fig.5.12.

Fig. 5.11: Linearised $t_{on}=f(V_{in})$.

Fig. 5.12: $V_{offset}=f(V_{in})$. 

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Correct division ratio, $n_{\text{offset}}$, can be found assuming that we already know one operation point of the converter: $V_o$, $V_{\text{in}}$, $t_{\text{off}}$, $t_{\text{on}}$ and $\tan(\alpha_{SG1})$. Crossing time, $t_c$ (Fig.5.13), can be calculated as follows:

$$t_c = t_{\text{off}} - t_{\text{on}}$$  \hspace{1cm} (5.13)

Offset voltage:

$$V_{\text{offset}} = \tan(\alpha_{SG1}) \cdot t_c$$  \hspace{1cm} (5.14)

And the division ratio:

$$n_{\text{offset}} = \frac{V_{\text{offset}}}{V_{\text{in}}}$$  \hspace{1cm} (5.15)
5.4 The calculated on-time reflection

Voltage slopes, $SG$, used in the circuit are generated by capacitors fed by constant current sources [G6]. In this case changing the charging current rate can easily change the angle of the slopes. This useful feature helps to overcome the restriction in the length of the reflected on-time.

Variation of $\alpha_{SG3}$ will lengthen or shorten the on-time referring to the calculated on-time. It can be used as an auxiliary regulation mechanism increasing flexibility of the control circuit, theoretically, $\alpha_{SG3}$, can change in the range:

$$\alpha_{SG2} < \alpha_{SG3} < 90^\circ$$

(5.16)

In practice the minimum $\alpha_{SG3}$ has to be bigger than $\alpha_{SG2}$, to cross over the slope $SG2$ in reasonable time, see Fig.5.14.

Fig. 5.14: Variable $\alpha_{SG3}$ illustration.
5.5 The output diode

The original flyback topology contains one diode at the output of the converter, for fast switching converters it is a Schottky diode.

A diode has a non-linear characteristic $i-v_F$, Fig.5.15 [G6]. Additionally the forward voltage drop decreases when the temperature rises (from $T_1$ to $T_2$). There is no simple way to create a highly accurate model of the diode on the primary side of the flyback converter. In our prototype we have assumed that $v_F$ is at constant level, Fig.5.15 ideal. This adds an additional error seen in the static characteristics for the load regulation, but it does not affect the control mechanism.

![Diagram of a diode and i-vp characteristics for two different temperatures, dashed line for an ideal case.](image)

Fig. 5.15: A diode and $i-v_F$ characteristics for two different temperatures, dashed line for an ideal case.

The diode used in the prototype is STPS20H100 and the forward voltage drop versus forward current can be seen in Fig.5.16. The assumed constant level was $v_F=0.4V$.

![Graph of forward voltage drop versus forward current, STPS20H100 [ST data sheet].](image)

Fig. 5.16: Forward voltage drop versus forward current, STPS20H100 [ST data sheet].
5.6 Synchronous rectifier for flyback converters.

The diode rectifier due to its forward voltage drop is the dominant loss component in power supplies with low output voltage [E5], [E9]. In this case the synchronous rectifier, SR, can be applied in such a power supply to reduce the conduction losses [A14]. Replacing the output diode with a low-on-resistance MOSFET reduces the rectification loss. A flyback converter with a SR is seen in Fig.5.17. In this case the SR’s MOSFET must be driven by a $V_{GS(SR)}$. This was discussed in details in [A14] for maximization of the conversion efficiency.

![Fig. 5.17: A flyback converter with a synchronous rectifier.](image)

However, in this work we are interested in some other advantages of using a MOSFET instead of the output diode. It is the $i_D-V_{DS}$ characteristic of MOSFETs. An example of the $i_D-V_{DS}$ of IRCZ44 MOSFET can be seen in Fig.5.18 [IRF data sheet]. It can be seen that for $V_{GS}=10\text{V}$ and $V_{GS}=15\text{V}$ the voltage drop is a linear function of the current. In this situation a mathematical model of the component on the primary side is easier to develop and better accuracy can be achieved when compared with the diode. Additionally temperature compensation is easier to achieve due to the resistive nature of the component in its on-state [G8]. In an ideal case we know the maximum current at the end of the on-time and the initial current on the secondary side, during the off-time, can be calculated.
Hence, the initial voltage drop across $R_{DS(SR)}$ can be found at the beginning of the off-time. The accuracy will improve but still will be limited by $R_{DS}$ differences within the same type of component.
Chapter 6

Extension to other control topologies

The proposed control strategy, based on the primary side calculated output voltage can be modified to achieve different solutions for the flyback converters. In this chapter we propose complete control circuits, including start-up circuits, with:

- Variable switching frequency (PFM)
  - Constant off-time with one slope implementation and with the peak detector reset at the end of the on-time.
  - Constant off-time with one slope implementation and with the peak detector reset at the beginning of the off-time.
  - Constant on-time and variable off-time.
  - Variable off-time and variable on-time, variable switching frequency.

- Constant switching frequency (PWM)
  - Controlled on-time and limited off-time
  - Controlled off-time and limited on-time

These circuits are examples of flexibility of the proposed control methodology together with the start-up circuit. They are the basis for further modifications during the design process to achieve a fully operating product.
6.1 Constant off-time with one slope implementation, reset at the end of the on-time

The previously proposed control methodology, Chapter 5 and § 4.2, is based on the on-time calculation during the off-time, Fig.4.8 and its reflection into the next operation cycle with two slopes, Fig.4.9. Nevertheless, different solutions with real time on-time calculation are possible, (see Fig.4.7.) and a solution with just one slope generator, SG1, is shown in Fig.6.1. In this case information from the peak detector output has to be available for longer than the off-time to be compared with SG1. Obviously this means that the peak detector reset must be placed somewhere else than during all the on-time. A possible solution is to place a constant peak detector reset pulse at the end of the on-time, after the comparison of SG1 and PD1, see Fig.6.1. In this case, the constant reset pulse determines the minimum on-time.

![Diagram](image)

Fig. 6.1: One slope implementation with the peak detector reset at the end of the on-time.

The proposed control circuit is shown in Fig.6.3. Eq.5.2 calculates the error voltage in this circuit in the traditional way. The on-time is calculated in real time by the direct comparison of the peak detector output signal with slope SG1. The error signal, as in circuit from Fig.5.2, after a gain $K_2$ is added with an offset voltage, $V'_{\text{offset}}$.

The offset voltage (feedforward regulation) is also calculated in a different way from $V_{\text{offset}}$ in circuit in Fig.5.2. For the minimum input voltage, $V_{\text{in} \text{min}}$, we need the maximum offset voltage, $V'_{\text{offset max}}$ and vice versa for the maximum input voltage, $V_{\text{in} \text{max}}$, minimum offset voltage is needed. This can be easily done with an additional subtracting circuit, Fig.6.2.
Where:

\[ V'_{\text{offset}} = (V_{\text{in max}} - V_{\text{in}}) \cdot n'_{\text{offset}} \]  

(6.1)

The correct division ratio, \( n'_{\text{offset}} \), can be found from Eq.6.1 assuming that we already know one operation point of the converter: \( V_o, V_{\text{in max}}, V_{\text{inn}}, t_{\text{off}}, t_{\text{on}} \) and \( \tan(\alpha_{SG1}) \), hence the offset voltage:

\[ V'_{\text{offset}} = \tan(\alpha_{SG1}) \cdot (t_{\text{on}} - t_{\text{reset}}) \]  

(6.2)

Fig. 6.2: The offset voltage, \( V'_{\text{offset}} \), calculation circuit.

The start-up circuit is exactly the same as presented in § 5.2. The description of the circuit shown in Fig.6.3 starts from the moment when the output voltage is greater than the Output voltage threshold, see Fig.6.4. Before SG1 was at maximum level (saturation level), Fig.6.4. (The following description of the control circuit operation is referred to Fig.6.3 and Fig.6.4).

When the first Constant off-time (2) starts, SG1 is reset by \( Q \) off-time (2). At the same time the peak detector reset signal is cancelled and the peak detector input signal is sensed. Before the peak detector was reset by Logic3 through TSB2.

When the Constant off-time2 is finishing then \( \bar{Q} \) off-time (2) is going high. This is the beginning of the on-time through TSB2. As a consequence Logic1 goes high too and after a time delay caused by invl&inv2 Logic2 is high also. Now Logic1 is high and waiting for the moment when the output of a comparator \( C_3 \) will go low.
The time delay between Logic1 and Logic2 (reset time delay, \( t_{dr} \)) is to create a time window for the peak detector reset pulse at the end of the on-time (Logic3 - NOR).

When \( C_3 \) is low then two things happen: 1) A reset pulse of the peak detector is starting, Peak d. reset. 2) Logic1 is going low. After some reset time delay, \( t_{dr} \), transition from high to low at the output of Logic2 triggers constant off-time(2) through TSB4.

The peak detector reset pulse is ended when \( Q \) off-time (2) is high and again the peak detector is ready to sense Peak d. input signal. The input signal appears after some time delay, \( t_d \), caused by components used. And all the operation cycle runs over again.

The circuit from Fig.6.3 has the same over current protection as the circuit described in § 5.1. When during normal cycle by cycle voltage mode control (not start-up current mode control) the primary side current is greater than Current limit level, \( I_p > I_{PL} \), then the on-time is finished immediately, see Fig.6.5. New constant off-time(2) is triggered by high-to-low transition at the output of Logic2, see waveforms in Fig.6.6. During constant off-time(2) the circuit is again in the normal operation mode. In this case, with the over current protection, reset of the peak detector is done by Constant reset-time (about 200ns) through TSB6. The reset is triggered by a high-to-low transition at the output of a comparator \( C_f \). This takes place at the beginning of the off-time.

From the design point of view it is important that Logic2 has to be high before the over current protection circuit is acting. This is not a problem in normal range of power, where the current limit is significantly bigger than zero. But it has to be taken into account in very low power applications. The reset time delay, \( t_{dr} \), and the current sensing resistor must be chosen carefully.
Fig. 6.3: Block diagram of the control circuit with one slope and the peak detector reset at the end of the on-time, together with the start-up circuit.
SQ^Si

Peak d. output
Peak d. input
Peak d. reset
Q reset-time=Y6
Q off-time (1)

* Q off-time (2) = SET(U2)
comparator C3 - output
Q' off-time(2)

Logic1
inv1
inv2
Logic2

on-time

* The first Q off-time (2) is triggered by Q (U^) when Vo>Vthr

△ Peak detector reset at the beginning of the off-time during start-up (current mode control)

△ Reset time delay, t_off, to reset the peak detector at the end of the on-time

Fig. 6.4: Signal waveforms of the control circuit from Fig.6.3, without over-current protection.

Fig. 6.5: Over current protection in the circuit from Fig.6.3.
The circuit proposed in Fig.6.3 operates in CCM and DCM. When compared with two slopes solution, § 4.2, it can be seen that here the number of slopes is reduced (from three to one). This may improve the accuracy and allows the on-time be longer than the off-time. But in this case we have one more constant pulse generator, *Constant reset-time*, and two extra buffers (*TSB*₂, *TSB*₃). Additionally we have a minimum on-time which can not be avoided in this circuit during normal operation. It is caused by the necessity of the peak detector reset. Nevertheless, a circuit proposed in the next paragraph, § 5.2, can overcome this limitation.

Fig. 6.6: Signal waveforms of the control circuit from Fig.6.3, with over-current protection.
6.2 Constant off-time with one slope implementation, reset at the beginning of the off-time.

An alternative solution for a real time on-time calculation with one slope proposed in § 6.1 is a circuit with the peak detector reset at the beginning of the off-time. A constant reset pulse starts immediately at the end of the on-time, see Fig.6.7. And is finished within the time delay of the signal between the switch voltage and the input signal of the peak detector. It is implemented in the circuit shown in Fig.6.8.

The offset voltage, $V_{\text{offset}}$, and the error signal, $V_{E}$, are calculated in the same way as before in § 6.1. And the start-up circuit is the same as presented in § 5.2.

![Fig. 6.7: One slope implementation with the peak detector reset at the beginning of the off-time.](image)

As before we start the description of the circuit, Fig.6.8, from the moment when the output voltage is greater than the output voltage threshold, see Fig.6.9 ($V_0>V_{\text{thr}}$). Before the slope $SG_1$ was at the maximum level and the peak d. output too, Fig.6.9. There were no reset signals during the start-up process. As a consequence $C_3$ output was high also. The first constant off-time, $Q_{\text{off-time}}$ (2), triggers a constant reset pulse, $Q_{\text{reset}}$ (3), and also resets $SG_1$. When $Q_{\text{reset}}$ (3) is finished the peak detector input signal is sensed and held until the next reset. $C_3$ output is high because $PD>SG_1$.

When constant off-time (2) is finishing then the on-time is starting, $\bar{Q}_{\text{off-time}}$ (2). The on-time is finishing when $C_3$ is going low ($GSI>PD$). The next off-time is triggered by Logic2 high to low transition.
During normal operation Logic2’s output depends on C3’s output (output of C1 is normally high). But the situation looks different when the over current protection circuit acts, Fig.6.10.

During the on-time SG1 is less than PD and C3 stays high, Fig.6.11. Now Logic2’s output depends on C1 output. When the primary side current is greater than the limit, \( I_p > I_{PL} \), then transition high to low at Logic2’s output triggers constant off-time (2) through TSB4. This resets SG1 and PD as described before.

The solution proposed in this paragraph is the simplest version of the primary side cycle-by-cycle voltage mode control circuit for flyback converters. Its natural limitation is the speed of components used. At this stage the circuit operates with the switching frequency in range of hundreds of kHz. There is not just the minimum on-time, but the minimum off-time is also always present. This is the time when the output voltage is calculated and processed on the primary side of the converter.
Fig. 6.8: Block diagram of the control circuit with one slope and the peak detector reset at the beginning of the off-time, together with the start-up circuit.
The first Q off-time (2) is triggered by Q (U^) when Vo>Vthr

* Peak detector reset at the beginning of the off-time triggered by constant off-time 2

---

Fig. 6.9: Signal waveforms of the control circuit from Fig.6.8, without over-current protection.

---

![Over current protection diagram](image)

Fig. 6.10: Over current protection in the circuit from Fig.6.8.
6.3 Constant on-time, variable off-time

6.3.1 Introduction

As a further extension of cycle by cycle control methodology for flyback converters we propose in this paragraph a circuit operating with constant on-time and variable off-time. But before we start to describe the circuit we will go through some analysis. This will help to understand better the circuit.

The idea of this control is shown in Fig.6.12. Now we have constant on-time and variable off-time. The off-time is changed by the peak detector output signal, PD1, compared with a slope SGI. The reset of PD1 and SGI takes place during the constant on-time.
The peak detector input signal and the offset voltage, $V_{\text{offset}}$, are calculated in the same way as in circuit shown in § 5.1. Now we explain why.

Let's first assume for a while that $V_{\text{in}}=\text{const}$, $\tan \alpha_{SG1}$ is known and the output voltage is changing. As a consequence $V_{\text{offset}}=f(V_{\text{in}})$ is a constant also. Now, if $V_o$ will increase then according to Eq.2.43 for CCM and Eq.2.50 for DCM the off-time must increase also to maintain the regulation. The off-time, $t_{\text{off}}$, will increase only when the peak detector output, $PD1$, will increase. In our control scheme $PD1=V_{\text{offset}}+V_E$, this means $PD1=\text{const}+V_E$. In this situation $V_E$ has to rise-up, so this is why we calculate the error voltage as $V_E=V_o-V_{\text{ref}}$. The same final result will be achieved for analysis when $V_o$ drops.

Now, let's change our initial assumptions to $V_o=V_{\text{ref}}$, $\tan \alpha_{SG1}$ is known and the input voltage is changing. As a consequence $V_E=0$ and $t_{\text{off}}=f(V_{\text{in}})$. So, if $V_{\text{in}}$ will drop then the off-time must decrease to maintain the regulation, it will happen only if the peak detector output decreases. With the present assumptions we have $PD1=V_{\text{offset}}+\text{const}$, this is why $V_{\text{offset}}$ must change in proportion to $V_{\text{in}}$, Eq.5.15. The same final result will be achieved for analysis when $V_{\text{in}}$ increases.

This analysis is right for an average mode control over many operation cycles. Now some additional analysis appropriate to cycle by cycle control scheme will be done.

If we are in CCM and $V_o$ suddenly (within one cycle) rises-up and $t_{\text{off}}$ also increases then the output voltage is rising even higher in the present cycle and in the next few cycles. Opposite situation: still in CCM, now when $V_o$ suddenly (within one cycle) drops and $t_{\text{off}}$ also decreases then the output voltage is dropping even faster in the next on-time or even in the complete next cycle (depending on the circuit conditions).
This is caused by the presence of RHPZ [G2], so in this situation a question must be asked - is this a desired solution for flyback converters? Answer is – it depends on the application, in general not.

If we assume now DCM and a sudden rise of $V_o$ and so $t_{off}$ then the desired regulation effect may be achieved in the next cycle. We will explain this with two examples.

**Example 1**

We are in DCM and the output current, $I_o$ has changed during the on-time of the first cycle from Fig.6.13. We assume that the error gain is low enough to cut-off the 1st cycle off-time in DCM, *DCM shorted by the control action*. This means that the off-time is shorter than it would originally have been, without the control action, but long enough to reach DCM.

![Diagram](https://via.placeholder.com/150)

Fig. 6.13: Constant on-time and variable off-time in DCM, the low error gain example.

In this case the primary side current in 2nd cycle again starts from the zero level. The output voltage during this on-time continues its drop. During the 2nd cycle off-time, $V_o$ rises-up but not enough to reach the reference level, $V_{ref}$, because the amount of energy
transferred was the same as in the 1\textsuperscript{st} cycle. The control action shorts DCM only. It will take more than one cycle to reach $V_{ref}$.

**Example 2**

We are again in DCM and as before, $I_o$ has changed during the 1\textsuperscript{st} on-time, Fig. 6.14, but now the error gain is high enough to cut-off the 1\textsuperscript{st} cycle off-time in CCM. This means that the off-time is finished before the secondary side current, $I_S$, reaches the zero level.

![Diagram of constant on-time and variable off-time in DCM, the high error gain example.](image)

Fig. 6.14: Constant on-time and variable off-time in DCM, the high error gain example.

As a consequence 2\textsuperscript{nd} cycle $I_P$ does not start from the zero level, more energy will be stored in the air gap of the flyback transformer. Obviously the output voltage drops during the on-time, but $V_o$ rises-up faster during 2\textsuperscript{nd} cycle off-time because of the larger $I_S$ (more energy transferred). In this case the output voltage may reach $V_{ref}$ in the next cycle (2\textsuperscript{nd} cycle) or even exceed it.

This is why the desired regulation effect may be achieved in the next cycle but may not always be. Theoretically the error gain can be large enough to ensure that $V_o$
will reach $V_{ref}$ in the next cycle but then there is a great danger that $V_o$ will significantly exceed $V_{ref}$. The off-time will increase to transfer all of the energy stored during the previous on-time (to reach DCM according to the control algorithm).

This control solution is probably the most inconvenient propose for flyback topologies, but from an analytical point of view this is an interesting case.

6.3.2 Proposed circuit operation theory

The proposed circuit is shown in Fig.6.16. Corresponding waveforms are shown in Fig.6.15. Description of the circuit will start from the moment when $V_o>V_{thr}$ (the end of the start-up process). During the start-up there is no reset of the peak detector. $SG1$ is also at its maximum level. The first constant on-time is triggered by the start-up circuit and next by a comparator, $C_3$, when $SG1$ is greater than Peak detector (1). The on-time pulse resets the peak detector and the slope $SG1$. The reset pulse of $SG1$ is also maintained for a while after the end of the on-time ($Constant time delay = t_{d_{max}}$), it is to ensure that $SG1$ will not start before the Peak detector (1) output signal.

Fig. 6.15: Signal waveforms of the circuit from Fig.5.16, without over current protection action.
In the situation when the over current protection circuit acts, $C_I$, the present on-time is cut-off instantly. It is done by the clear signal applied to the Constant on-time generator (clear active when logic low applied). The general idea is shown in Fig.6.17. Detailed waveforms can be seen in Fig.6.18.
Fig. 6.16: Block diagram of the control circuit with constant on-time and variable off-time, together with the start-up circuit.
Fig. 6.17: Over current protection action in the circuit from Fig.6.16.

The circuit presented in this paragraph is probably the least component circuit for the control, but as mentioned in § 6.3.1 this approach by the definition causes some difficulties [G14]. The suggested operation mode is DCM. There is also the minimum off-time necessary to maintain the regulation.
6.4 Variable off-time and variable on-time, variable frequency Control

The last topology for variable frequency flyback converters is based on control of the on-time and the off-time in each operation cycle. This means variable on-time and variable off-time. The proposal here is a combination of the circuits from § 6.2 and § 6.3. A simplified block diagram is shown in Fig.6.21. Block called $V_o$ calculation can be easily reconstructed from the previous circuits in this chapter or from the original circuit presented in § 5.1. Block called Start-up circuit is the same as discussed in § 5.2.

As it can be seen in Fig.6.21, there are two main regulation (or control) paths. The first one with a peak detector $PD1$ is dedicated to the off-time control. The second one with a peak detector $PD2$ is dedicated to the on-time control.

A basic idea of this control approach is shown in Fig.6.20. Detailed waveforms are a combination of those from § 6.2 and § 6.3. Peak detectors, $PD1$ and $PD2$, have the same reset signal, $const.\ pulse_2$, at the beginning of the off-time. The reset pulse, $resetPD1 \& resetPD2$, must be shorter than the maximum time delay, $t_{d_{max}}$. This is to minimise the minimum necessary off-time and to avoid the situation when $SG1$ starts before $PD1$ output signal.

There must be a reserved time, Peak detection area, when the peak detectors senses the input signals. $SG1$’s reset, $resetSG1$, is a combination of $t_{d_{max}}$ and the on-time ($logic_3$). $SG2$’s reset is the off-time.

The off-time is finished, $reset1$, when $SG1$ is bigger than $PD1$’s output ($C_{off}$ comparator), but only if $SG1$ was bigger than the zero level (ensured by $logic1$). The on-time is finished when $SG2$ is bigger than $PD2$’s output ($C_{on}$ comparator).

The over-current protection is provided by $C_l$ and $logic2$. The on-time is cut-off when $I_P>I_{PL}$. 

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Fig. 6.20: General idea of independent regulation of the on-time and the off-time of flyback converters.

The circuit presented in this paragraph combines the best features of variable frequency, cycle by cycle control approach in flyback converters. Dynamic performance of the proposed circuit can be compared only with the hysteretic controller for forward converters [G7]. But our circuit additionally provides galvanic isolation, it is fundamentally a primary side controller.
Fig. 6.21: A block diagram of the control circuit for flyback converters with variable on-time and variable off-time.
6.5 Constant switching frequency

Power converters have to meet EMC requirements [G1]. The dominant source of EMI problems is the switched current waveform [G7], [G1], [G3]. To meet limits in conducted EMI, a filter must be added at the power input of a switching converter. In case of EMC sensitive applications, a constant switching frequency approach reduces the input filter complexity significantly. The cycle by cycle control methodology can be extended to such a sensitive applications.

The constant frequency topology can be achieved easily after some modifications of the circuits proposed in this chapter for variable frequency. Generally, there are two possible options.

- **Controlled on-time and limited off-time**, Fig.6.22 Option 1. The on-time is triggered by the falling slope of a clock signal, Clock end is ended when a slope is greater than a peak detector output and the off-time is used for the rest of the constant period, $T$ (suitable circuits § 6.1 and § 6.2 or § 6.4).

- **Controlled off-time and limited on-time**, Fig.6.22 Option 2. The off-time is triggered by the falling slope of a clock signal, Clock and is ended when a slope is greater than a peak detector output and the on-time is for the rest of the constant period, $T$ (suitable circuits § 6.3 or § 6.4).

![Fig. 6.22: General control mechanisms for constant frequency flyback converters.](image_url)

As an example, we show a solution for Option 2. A modified circuit from § 6.4 is shown in Fig.6.23. The on-time regulation patch was deleted and two additional components were added. Clock is to set the constant switching frequency. Const. pulse4 is to ensure that after $C_4$ action there will be no second on-time pulse within the same period. The circuit shown in Fig.6.23 is not an optimal solution and further modifications (optimisation) can be done.
Fig. 6.23: Block diagram of a circuit with a constant switching frequency, the off-time triggered by a clock pulse.
Chapter 7
Design of the Circuit

This is the stage when all the information about the new control mechanism is gathered together and the first prototype can be built. The general strategic decisions about the circuit configuration have been made. Now is the time to make decisions about details of the physical components of the circuit. These decisions are based on design calculations, available technology and components data sheets, design experience and consultations with other design engineers.

The design calculations give the criteria for the components selection. At this stage the design experience of other experts in the field can substantially reduce the complexity of calculations and the development time. Experience helps to find a compromise between sufficiently good accuracy and possible high accuracy of formulas used.

Once the criteria for components are known we can start to look for them. Nowadays there are lots of facilities in this research and the main ones are:

- Internet search engines
- Manufacturer data books
- Personal contacts with components distributors

An important aspect is the substrate for all the circuit. In our case we use discrete components and the most convenient substrate is a printed circuit board (PCB). In our prototype we use FR4 [G11], it is made of fibreglass and resin.

In this chapter we present the design of the power stage, the voltage recovery circuit, the control circuit and discussion about layout of the PCB.
7.1 Design of the power stage

The power stage of a flyback converter consists of the main flyback transformer, the main switch on the primary side, the output diode and the output capacitor (and the input filter capacitor). In this chapter a complete design procedure with the components selection is shown.

The design specification is as following:

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range:</td>
<td>$V_{inmin}=16V$, $V_{inmax}=24V$,</td>
</tr>
<tr>
<td>Efficiency of the converter:</td>
<td>$\eta=70%$</td>
</tr>
<tr>
<td>Minimum switching frequency:</td>
<td>$f_{smin}=100kHz*$</td>
</tr>
<tr>
<td>Output voltage = reference:</td>
<td>$V_o=3.3V$</td>
</tr>
<tr>
<td>The maximum output current:</td>
<td>$I_{omax}=1.2A$</td>
</tr>
</tbody>
</table>

*This is for an ideal case when $t_{onmax}=t_{off}$. In reality $t_{on}<t_{off}$ (§ 10.1), we assume that $t_{on}=0.95*t_{off}$, so for constant off-time, $t_{off}=5\mu s$, the maximum on-time is $t_{onmax}=4.75\mu s$.

The input and the output voltage ripple are not defined in this case. This is an experimental prototype and values of the input and the output filter capacitors will change.

Calculations:

<table>
<thead>
<tr>
<th>Name</th>
<th>Equation:</th>
<th>Value:</th>
</tr>
</thead>
<tbody>
<tr>
<td>The output power:</td>
<td>$P_o = V_o \cdot I_{omax}$</td>
<td>$P_o=3.96W$</td>
</tr>
<tr>
<td>The input power:</td>
<td>$P_{in} = \frac{P_o}{\eta}$</td>
<td>$P_{in}=5.657W$</td>
</tr>
<tr>
<td>Primary side max. average current:</td>
<td>$I_{pmax Avg} = \frac{P_{in}}{V_{in min}}$</td>
<td>$I_{pmax Avg}=0.354A$</td>
</tr>
</tbody>
</table>
Primary side peak current boundary coefficient:

\[ k_{pp} = \frac{2 \cdot (t_{on\max} + t_{off})}{t_{on\max}} \]

\[ k_{pp} = 4.105 \]

Primary side peak current, boundary condition:

\[ I_{pp} = k_{pp} \cdot I_{pmax\ Avg} \]

\[ I_{pp} = 1.452A \]

\[ i_p \text{ slew rate:} \]

\[ \frac{di_p}{dt} \Rightarrow \frac{\delta i_p}{\delta t} \Rightarrow \frac{I_{pp}}{t_{on\max}} \]

\[ I_{pp}/t_{on\max} = 305.6k \text{ A/s} \]

Primary side critical inductance:

\[ L_{mcrit} = \frac{V_{in\ min}}{I_{pp}} \cdot \frac{I_{pp}}{t_{on\ max}} \]

\[ L_{mcrit} = 52.36 \mu H \]

When voltage is applied to the primary side during the on-time, energy is stored in the magnetic field and the input current increases linearly at the rate of \( \frac{di}{dt} = \frac{e}{L} \). The energy stored will be \( \frac{1}{2}L_i^2 \) and multiplying this by the frequency will give the power throughput.

Check of the maximum power throughput:

\[ P_T = \frac{1}{2} \cdot L_{mcrit} \cdot I_{pp}^2 \cdot f_{s\ min} \]

\[ P_T = 5.657W \]

To ensure “early” CCM with this inductor we set \( L_m = 55 \mu H > L_{mcrit} \).

Flyback transformers are not transformers, but multi-winding inductors and have to be designed as such. The rectifier diode on the output side is phased such that when current flows in the winding on the primary side, there is no current in the secondary side and vice versa. Therefore all the energy for the outputs must be stored in the magnetic circuit from one half cycle to the next. Since there are no secondary ampere-turns to cancel the primary ampere-turns, it is clear that there is a very significant magnetising force on the core and it is necessary to include an air-gap to stop saturation. Assuming that for the core with an air-gap the core reluctance, \( R_c \), is negligible when compared with the air-gap reluctance, \( R_g \), [G1] can be written:
where: \( N_p \) is number of the primary turns, \( A_c \) is a cross section area of the core, \( \mu_o \) is the permeability of free space \((4\pi\times10^7 \text{ H/m})\) and \( l_g \) is the air gap length. The air-gap length can be calculated from Eq.7.1 once all elements of the equation are known.

At this stage the magnetic core can be found. For purpose of the prototype we assume that \( \delta B = 0.5\times B_{sat} \) of a ferrite core [G7]. With this assumption we do not fully utilize the magnetic core but the safety margin is bigger. In case of a commercial design it could be around 70%, not only 50%. Now from a catalogue \( B_{sat} \) of a core must be chosen. In our case we use PC 50 EPC 19-Z [H1]. \( B_{sat}=440\text{mT at 60°C} \). Rearranging Eq.7.2 the cross section area \( A_c \) can be calculated, but we also must decide now about the number of secondary turns.

\[
\delta B = \frac{V_{in\min} \cdot T_{on\max}}{N_p \cdot A_c} \quad (7.2)
\]

For \( V_o=3.3\text{V}+1\text{V} \) let the secondary be \( N_s=5 \) turns, so the secondary volts per turn \( V_{PT_{sec}}=4.3/5=0.86\text{V/turn} \). Now the primary number of turns can be calculated. But before it will be done, we will clarify something. [G7] Let us assume that we have the primary and secondary volts/turn identical and operating in discontinuous mode. Now let us choose to decrease the secondary turns. The volts/turn on the secondary will now be higher than that on the primary, since the output voltage stays constant. During the off-time, the secondary voltage will be reflected onto the primary by the ratio of the number of turns, so it will be higher than before. To maintain equal volt-seconds on the primary, the on-time will increase and the off-time decrease. Another effect will be that the \( \delta i/\delta t \) will be higher during the off-time than the on-time, this is due to the same voltage, but smaller inductance (reduced turns) on the secondary therefore, the flyback time will always be shorter than the on-time. Since the maximum (ideal) on-time is 50%, there will always be enough time for the inductor current to get down to zero before the end of the off-time. Care must be taken to make the inductance high enough such that enough energy is stored in the half cycle, otherwise the outputs will collapse.
Alternately, advantage can be taken of this in-built, free and automatic power limit facility.

Had we chosen to round up the secondary turns and thus made the primary volts/turn more than that of the secondary, the flyback time will be longer than the on-time and so there may be some inductor current at the end of the cycle. This results in a continuous, trapezoidal current waveform or continuous mode operation. Under these conditions there is no automatic power limiting. These characteristics are shown in the table below:

| Table 7.1 \( L_m \) versus \( L_{mcrit} \) and \( VPT_{prim} \) versus \( VPT_{sec} \) |
|-----------------|-----------------|-----------------|
| \( VPT_{prim} < VPT_{sec} \) | \( VPT_{prim} > VPT_{sec} \) |
| \( L_m > L_{mcrit} \) | Power limiting | Continuous |
| \( L_m < L_{mcrit} \) | Discontinuous | Discontinuous |

Note that if cont. op. is disabled, power limiting will occur if the inductance is higher than critical. (the average input current is insufficient to power the load)

Fig. 7.1: Primary current waveforms for different primary inductances.

In our design it is not our intention to operate in CCM only but in DCM mainly with an option of the boundary operation and “early” CCM. That is why we have set the magnetizing inductance a little bigger than \( L_{mcrit} \) and now we set \( VPT_{prim} = 1V/\text{turn} > VPT_{sec} = 0.86V/\text{turn} \).
The primary number of turns:

\[ N_p = \frac{V_{in\min}}{V_{PT\ prim}} \]

\[ N_p = 16 \]

Cross section area:

\[ A_c = \frac{V_{in\min} \cdot t_{on\max}}{N_p \cdot \delta B} \]

\[ A_c = 21.6 \text{ m}^2 \]

And for PC 50 EPC 19-Z \( A_c = 22.7 \text{ mm}^2 > 21.6 \text{ mm}^2 \).

The AC Flux density:

\[ \delta B = 220 \text{ mT} \]

The air-gap length:

\[ l_g = \frac{N_p^2 \cdot A_c \cdot \mu_o}{L_m} \]

\[ l_g = 1.328 \times 10^{-4} \text{ m} \]

As we said before there is “early” CCM operation allowed. In this situation it is necessary to check if the total flux density, \( B_T \), does not exceed \( B_{sat} \). To calculate \( B_T \) we must know \( B_{DC} \). Here we use \( I_{p \ max \ Avg} \). This current is much higher than unknown current possible in CCM, so if \( B_T < B_{sat} \) then it is ok.

DC flux density:

\[ B_{DC} = \frac{\mu_o \cdot I_{p \ max \ Avg} \cdot N_p}{l_g} \]

\[ B_{DC} = 54 \text{ mT} \]

Total flux density:

\[ B_T = \delta B + B_{DC} \]

\[ B_T = 274 \text{ mT} < B_{sat} \]

The core loss according to the date sheet for the chosen core is \( P_c = 0.084W \).

The wire gauge was selected according to [G3], [G7] (skin and proximity effect at 100kHz) and is #27 (0.361mm) for the primary and the secondary side. Both windings are quadfilar. The bobbin type for the select core is BEPC-19-1111 CPH [H1].
Table 7.2 The transformer design summary.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic core</td>
<td>PC 50 EPC 19-Z</td>
</tr>
<tr>
<td>Bobbin</td>
<td>BEPC-19-1111 CPH</td>
</tr>
<tr>
<td>Air gap</td>
<td>1.328*10^4 m</td>
</tr>
<tr>
<td>Primary winding</td>
<td>16 quadfilar turns, gauge #27</td>
</tr>
<tr>
<td>Secondary winding</td>
<td>5 quadfilar turns, gauge #27</td>
</tr>
</tbody>
</table>

The primary side MOSFET voltage:

\[ V_{DS_{\text{max}}} = V_{in_{\text{max}}} + \frac{N_p}{N_s} \left( V_o + 1 \right) \]

\[ V_{DS_{\text{max}}} = 37.76V + \text{spikes} \]

MOSFET IRFR 110 was chosen as the primary switch. The secondary side diode is a dual Schottky S6/100. The switch and the diode were chosen according to the manufactures data sheets.

7.2 The output voltage calculation on the primary side circuit

In this paragraph we describe the design of the electronic control circuit. The circuit calculates the output voltage on the primary side of the converter during the off-time according to Eq.3.9. The schematics of the circuit with the components values are shown in Appendix 3 and the following description of the circuit is referred to them. We discuss in this paragraph only the major significant values component values and neglect the more obvious ones e.g. high frequency voltage dividers (with the coupling capacitors), in this case we talk only about the division ratio. The filter capacitors on the supply line off the IC and associated components are also not discussed, they are specified in the component’s data sheet. The data sheets of all the components used in the circuit are available through the Internet or from the distributors.

The switch voltage is sensed across the main switch, Q2, with its damping network, \((R7, C33)\), discussed in §3.2.1. This voltage is divided by 20, \((R10, R9, R8, \text{ and } C34)\), to be within the common mode input voltage range of the components used. After the voltage divider is buffered, \((CLC111; U25)\). The input voltage is also divided.
by 20, \((R2, R3, R4, \text{and} \ C18)\), for the same reason as the switch voltage and buffered \((CLC; \ U28)\). Output signals of \(U25\) and \(U28\) are fed to \(U10\) \((EL4430)\), where they are subtracted. The signal at the output of \(U10\) is limited, \(>0\), (prevented from going negative value during the on-time) by a diode-limiting network \((BAT\ 54, \ CR2)\). The signal obtained is fed through a buffer, \(U26\), to a voltage divider, \((R14, R15, R16, \text{and} \ C38)\). This voltage divider represents the inverted transformer turns ratio, \(N_t/N_p\). From this signal the forward voltage drop of the output diode is subtracted. It is done in \(U11\), \((EL4430)\). The forward voltage drop of the diode is assumed as a constant value, \(V_f=0.6V\). The output signal of \(U11\) is the calculated output voltage divided by 20. This signal is buffered, \(U27\), and fed to \(U3\) \((CLC449)\).

7.3 From the error voltage calculation to the peak detection circuit

\(U3\) is a non-inverting amplifier, with the gain equal to 10. At the output of \(U3\) (across \(R23\)) half of the output voltage is obtained. The calculated output voltage contains the initial transient spike, which is not damped by the damping network. The spike is removed by a low pas filter network \((R56 \text{and} \ C41)\). The calculated output voltage is fed to \(U12\), \((EL4430)\). The reference voltage, \(E10, (V_{ref}=1.65V)\) is also fed to \(U12\) and subtracted there from the calculated input voltage. The result in the error signal is obtained at the output of \(U12\). The error signal through the buffer \(U29\), is fed to an non-inverting gain amplifier, \(U4\) \((CLC449)\). The gain was set experimentally to 10, \((R28, R29 \text{and} \ R30)\). The amplified error signal is fed to a limit network \((CR4 \text{and} \ CR3)\), through a filter \((R57 \text{and} \ C43)\) and a buffer \(U30\). The filter is the same as before \(U12\), \((R56 \text{and} \ C41)\). The limits are +/- 1.2V, \((E11=0.8V \text{and} \ E12=-0.8V)\). The limited signal is buffered by \(U31\).

The output signal of \(U31\) is added to the offset voltage in \(U13\). The offset voltage in this circuit was applied externally, \(E13=-1.42V\) for \(V_{in}=20V\), calculated in § 5.3 after SG1 calculation. At this stage the circuit can sense its maximum value, this is done by the peak detector, analyzed and described in details in Chapter 8. The peak detector reset signals comes from the control part of the circuit, described in § 5.1, and is the same as the on-time.
7.4 Auxiliary circuit parts—excluding start-up

The output signal from the peak detector, \(U_{36}\), is sent to the negative input (Pin 2) of a comparator \(U_{15}\) (LT1015), where it is compared with a slope (SG1 Pin 3, § 4.2). As a result of the comparison the calculated on-time is obtained.

Before we go further, we show the SG1 calculation together with \(V_{\text{offset}}\). SG1 voltage ramp (Fig.4.9, § 4.2) created by capacitor, \(C_{29}\), charged from a constant current source, with a reset capability. The constant current is supplied from a current mirror [G6], \((U_9, BCV62\) and resistors \(R_{46}, R_{51}\)). The reset is done by a MOSFET, \(BSS138\), controlled by the on-time signal. \(U_9\) is supplied by the logic output of \(U_{20}\) (Pin 11, 5V) during the normal operation’s off-time (not during the start-up).

**SG1 Input parameters:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(U_{20}) supply voltage:</td>
<td>(V_{ccSG1}=5V)</td>
</tr>
<tr>
<td>SG1 amplitude:</td>
<td>(V_{SG1\text{max}}=3V)</td>
</tr>
<tr>
<td>CSG1 is capacitor’s (C_{29}) value:</td>
<td>(CSG1=1.2nF)</td>
</tr>
</tbody>
</table>

**SG1 calculation:**

<table>
<thead>
<tr>
<th>Name</th>
<th>Equation</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSG1 is a sum of (R_{46}) and (R_{51}):</td>
<td>(R_{SG1} = \frac{V_{ccSG1} \cdot t_{off}}{V_{SG1\text{max}} \cdot C_{SG1}})</td>
<td>(R_{SG1}=6.94k\Omega)</td>
</tr>
<tr>
<td>The nominal input voltage:</td>
<td>(V_{in\text{nom}} = \frac{(V_{in\text{max}} - V_{in\text{min}})}{2} + V_{in\text{min}})</td>
<td>(V_{in\text{nom}}=20V)</td>
</tr>
<tr>
<td>(t_{on}=f(V_{in\text{nom}}, V_{o})):</td>
<td>(t_{on} = \frac{N_p}{N_S} \cdot \frac{V_o}{V_{in\text{nom}}} \cdot t_{off})</td>
<td>(t_{on}=2.64\ \mu s)</td>
</tr>
<tr>
<td>Cross over time, (§ 5.3, Eq.5.13):</td>
<td>(t_c = t_{off} - t_{on})</td>
<td>(t_c=2.36\ \mu s)</td>
</tr>
<tr>
<td>(\tan(\alpha_{SG1})):</td>
<td>(\tan(\alpha_{SG1}) = \frac{V_{ccSG1}}{R_{SG1} \cdot C_{SG1}})</td>
<td>(\tan(\alpha_{SG1})=0.6*10^6)</td>
</tr>
<tr>
<td>The nominal offset voltage:</td>
<td>(V_{\text{offset}}=\tan(\alpha_{SG1}) \cdot t_c)</td>
<td>(V_{\text{offset}}=1.42V)</td>
</tr>
<tr>
<td>The offset division ratio:</td>
<td>(n_{offset}=\frac{V_{\text{offset}}}{V_{in}})</td>
<td>(n_{offset}=0.071)</td>
</tr>
</tbody>
</table>
In the circuit $R46 = 6.8k\Omega$ and $R51 = 500\Omega$ (variable resistor). The same components’ values are in the circuit where ramp SG2, ($R48$ and $R53$), is generated. The ramp GS3 rises-up with double speed, §5.4, so the current programming resistor is half of that in SG1 or SG2, $R47 = 3.3k\Omega$ and $R52 = 500\Omega$ (variable resistor).

Once we have calculated the on-time, it can be reflected into the next operation cycle as the main MOSFET’s, $Q2$, driving signal. It is described in § 4.2 and § 5.4 with details and the circuit is done with $U7$ as SG2, $U8$ as SG3 and a comparator $U16$ ($LT1015$).

$U7$ is supplied by $U23$ which is the OR gate. This gate provides the supply signal through the boundary between the present off-time and the next on-time. It is the OR function of signals from $U20$ (Pin 3) and $U24$, (Pin 2), where $U24$ is the inverted off-time. The reset of SG2 is the $U23$ inverted by $U24$, (Pin 4). $U8$ is supplied by the output of $U24$, (Pin 2) and is reset by the off-time.

When SG3 is bigger than SG2, the $U16$ goes “low” and through $U2$ the signal is sent into the start-up circuit. This signal after a buffer, $U34$, is also used to reset the peak detector, $Q3$ ($BSS138$).

The start-up circuit, described in details in § 5.2, sends the signal from $U2$ to the constant off-time generator $U14$, (HEF 4528, Pin 11) through:

- $U19$ (input Pin 5, output Pin 6) – this is TSB2 in Fig.5.5, § 5.2,
- $U20$ (input Pins 4 and 5, output Pin 6) – this is the signal conditioning AND gate,
- $U19$ (input Pin 12, output Pin 11) – this is TSB4 in Fig.5.5, § 5.2,
- $U21$ (input Pins 10 and 9, output Pin 8) – this is the signal conditioning AND gate.

The output signal from $U14$, (Pin 10) is send to a voltage divider, ($R89$, $R90$ and $C89$), to reduce the voltage from 10V to 5V, and after is sent through a buffer, $U35$, to the control circuit as the main off-time, set by $R85$ and $C30$. The first signal from $U14$ (Pin 10) is also sent through the conditioning AND gate, $U20$ (output Pin 8) to $U6$, (Pin 9) to switch off the start-up circuit.

$U2$ is a three input AND gate, where:

- Pin 1 is the over-current protection signal, normally “high” from a comparator $U17$ ($LT1015$),
- Pin 2 is the output of $U16$,
- Pin 13 is the inverted off-time from $U24$ (Pin 2), to ensure that there is no “high” output at Pin 12 during the off-time.
The reflected on-time from \( U20 (Pin\ 6) \) is also sent to \( U22 (MIC\ 4427) \), which is the main MOSFET driver.

### 7.5 The start-up circuit

The start-up circuit is described in details in § 5.2. In this section we only present a list of equivalent components between the schematic in Appendix 1 and the block diagram Fig.5.5 in § 5.2. The constant off-time is the same as for normal operation and is set by \( R41 \) and \( C53 \). The start-up off-time is fed into the circuit through a voltage divider, \((R42, R43\) and \( C55)\), to reduce 10V to 5V.

The current sensing resistor, \( R6 \) is a parallel combination of four 6Ω surface mounted resistors, 1% tolerance.

<table>
<thead>
<tr>
<th>Schematic in Appendix1 part:</th>
<th>equivalent</th>
<th>Part in Fig.5.5:</th>
</tr>
</thead>
<tbody>
<tr>
<td>( U14,\ Pin\ 5 )</td>
<td></td>
<td>Constant off-time (1)</td>
</tr>
<tr>
<td>( U14,\ Pin\ 7 )</td>
<td></td>
<td>Constant off-time O</td>
</tr>
<tr>
<td>( U17 )</td>
<td></td>
<td>C1</td>
</tr>
<tr>
<td>( U18 )</td>
<td></td>
<td>C2</td>
</tr>
<tr>
<td>( U21,\ Pin\ 3 )</td>
<td></td>
<td>initial reset</td>
</tr>
<tr>
<td>( U21,\ Pin\ 6 )</td>
<td></td>
<td>initial set</td>
</tr>
<tr>
<td>( U5 )</td>
<td></td>
<td>U1</td>
</tr>
<tr>
<td>( U6 )</td>
<td></td>
<td>U2</td>
</tr>
<tr>
<td>( U19,\ Pin\ 2\ and\ Pin\ 3 )</td>
<td></td>
<td>TSB1</td>
</tr>
<tr>
<td>( U19,\ Pin\ 5\ and\ Pin\ 6 )</td>
<td></td>
<td>TSB2</td>
</tr>
<tr>
<td>( U19,\ Pin\ 9\ and\ Pin\ 8 )</td>
<td></td>
<td>TSB3</td>
</tr>
<tr>
<td>( U19,\ Pin\ 12\ and\ Pin\ 11 )</td>
<td></td>
<td>TSB4</td>
</tr>
</tbody>
</table>
7.6 PCB layout

Printed Circuit Board (PCB) for the final prototype, together with schematics and components placement are shown in Appendix 3. The author, in cooperation with Artesyn Technology’s PCB designers, has designed it. Three additional circuits preceded the final prototype.

The first circuit was manufactured with wire connections, on a strip board, (see Appendix 5, Fig.A5). It was a circuit mainly with constant current sources, fast comparators and digital components. The idea of signal reflection with two slopes was tested there.

Second board, was a PCB for the output voltage calculation on the primary side, see picture in Appendix 4, Fig.A4.

Third PCB was developed for a fast peak detector and can be seen as a smaller PCB in Fig.A4, Appendix 4.
Chapter 8
Peak Detector Circuit

Cycle by cycle primary side controlled flyback converter works in continuous and discontinuous conduction mode. In order to provide control signal to the primary switch in each operation cycle, it is necessary to design a peak detector to hold the initial voltage after the switch closes. This will ensure that the circuit can work in both continuous and in discontinuous modes of operation for the flyback converter. To obtain high precision, it must be an active peak detector [G12].

8.1 Theory of operation of a peak detector

A diode and capacitor are the principle elements of a peak detector circuit, (see Fig.8.1). Ideally the capacitor, C, in Fig.8.1 will hold the diode's output voltage, $V_o$, at the most positive value attained by the input, $V_{in}$. In reality this topology suffers because of the forward voltage drop, $V_F$, of the diode and the diode leakage during the holding state.

![Fig. 8.1: Basic idea of peak detection.](image)

In order to be able to precisely rectify signals, it is necessary to reduce $V_F$. Basically this can be achieved by using a precision rectifier circuit (see Fig.8.2 and waveform), called a "superdiode". The diode in the feedback-loop of the amplifier, $A$, compensates for $V_F$. The output voltage, $V_o$, is equal to the positive input voltage, $V_{in}$. 
because the feedback mechanism it sets the amplifier output voltage, \( V_{oa} \), at one diode drop above the input voltage.

Replacing the diode in Fig.8.1 with the “superdiode” we obtain the basic active peak detector shown in Fig.8.2. Operation of the circuit follows from the fact that if \( V_{in} > V_o \), the op-amp output, \( V_{oa} \), is positive, so that diode \( D \) conducts. The capacitor, \( C \), is then charged through \( D \) (by the output current of the amplifier) to the value of the input because the circuit is a voltage follower.

![Fig. 8.2: Forward voltage drop of the diode (\( V_F \)) compensation – “superdiode”.

Fig. 8.2: Forward voltage drop of the diode (\( V_F \)) compensation – “superdiode”.

When \( V_{in} \) falls below the capacitor voltage, the op-amp goes negative to the saturation level and the diode becomes reverse-biased. Thus the capacitor gets charged to the most positive value of the input.

![Fig. 8.3: Precision peak detector.

Fig. 8.3: Precision peak detector.

When the peak detector is required to hold the value of the peak precisely, the capacitor must be buffered, as shown in Fig.8.3. Here op-amp \( A_2 \) (high input impedance and low input bias current) is connected as a voltage follower. Diode \( D_1 \) is the essential
diode for the peak-rectification operation. Diode $D_2$ prevents negative saturation and the associated delays of op-amp $A_1$. During the holding state, follower $A_2$ supplies $D_2$ with a small current through $R_I$. The output of op-amp $A_1$ will then be clamped at one diode drop below the input voltage. If the input $V_{in}$ increases above the value stored on $C$, which is equal to the output voltage, $V_o$, op-amp $A_1$ sees a net positive input that drives its output toward the positive saturation level and turns off diode $D_2$ (as $V_o$ gets closer to $V_{in}$, $A_1$ operates in linear mode). Diode $D_I$ is then turned on and capacitor, $C$, is charged to the new positive peak of the input. After that time the circuit returns to the holding state.

The circuit in Fig.8.3 has also the reset switch $Q$. The switch is activated by an external signal. The component $Q$ has to be a low-leakage switch otherwise it is necessary to deal with the reset switch leakage. It can be solved using the circuit shown in Fig.8.4. The switch can be implemented with two n-channel MOSFETs. Applying a positive-going pulse to the gates, $V_G$, turns both transistors on and discharges the capacitor, $V_c$, to ground. Upon removal of the reset pulse, the transistors go off. Because of the presence of $R_2$ and the voltage follower $A_2$, the voltage drop across $Q_I$'s channel is maintained essentially at zero, thus eliminating leakage through $Q_I$. The leakage of $Q_2$ is absorbed by $R_2$. In practice, when the holding time is less than a few microseconds the low leakage MOSFET switch is good enough.

![Fig. 8.4: MOSFET's leakage elimination.](image)

**8.2 Minimising the leakage current in the diode**

A similar technique can be applied to minimise leakage through the diode. When reverse-biased, a diode exhibits a leakage current, which also doubles with about every 10°C of temperature increase. A solution for this problem is shown in Fig.8.5. The
circuit achieves zero leakage current by maintaining 0 V across the diode, \( D_3 \) when it is in the "off" state. At the arrival of a new peak both \( D_1 \) and \( D_3 \) turn on, charging \( C \). \( V_{o1} \) must go now two diode drops above \( V_C \). This is not a problem as long as \( A_1 \) is below positive saturation level. After the peak, \( D_1 \) is reverse-biased and \( D_3 \) is held essentially at zero bias by \( R_2 \), which pulls \( D_3 \)'s anode to \( V_o \). This is the same voltage as that of the cathode. In practice, \( D_3 \)'s bias will not be exactly zero, this is because of the \( A_3 \)'s input offset voltage and the small voltage drop on \( R_2 \) caused by leakage of \( D_1 \) [G12].

![Diagram of diode leakage compensation](image)

Fig. 8.5: Diode leakage compensation.

### 8.3 Speed and accuracy issues

A serious source of quality degradation is the storage capacitor. Capacitors exhibit a leakage current, which tends to slowly discharge them. Usually it is considered as an equivalent parallel resistance. Additionally dielectric absorption must be taken into account [G12]. This causes a "sagback" effect after a sudden change in the capacitor voltage, \( V_C \). It can be modelled as an internal \( R_D-C_D \) network in parallel with \( C \), see Fig.8.6. When the discharging switch \( Q \) goes on the capacitor will discharge instantaneously, however, \( C_D \) will retain some charge due to the \( R_D \). After \( Q \) is off, some energy will be transferred from \( C_D \) to \( C \) in order to achieve voltage equilibrium, which causes the "sagback" effect. Solutions for this problem are very low leakage and low dielectric absorption capacitors, like polystyrene and teflon.
When the peak detector holding time must be very long it is necessary to take into account all possible leakage in the circuit. Apart from these mentioned above, printed circuit board leakage must be considered. It can be solved by miscellaneous PCB design solutions, which are not discussed here. The smaller the leakage current, the better the peak detector performance. The voltage drop along with time ($\Delta V_c/\Delta t$ [V/sec]) is directly proportional to the leakage current ($I_{lk}$ [A]), Eq.8.1.

$$\frac{\Delta V_c}{\Delta t} = \frac{I_{lk}}{C}$$

(8.1)

Another important issue to discuss is the speed capability of the peak detector. It depends on the maximum rate at which $C$ can be charged. From the widely known equation (Eq.8.2) it can be seen that for large values of $C$, the speed is limited by the $A_I$ output current capability ($I_{oI(max)}$). For small values of $C$, speed of the circuit is limited by the slew rate of $A_I$, Eq.8.3. Diodes' speed is not an issue as long as we use Schottky diodes, otherwise it is necessary to check forward recovery time in the data book.

$$\left.\frac{dV_c}{dt}\right|_{max} = \frac{I_{C(max)}}{C} \Rightarrow \frac{I_{oI(max)}}{C}$$

(8.2)
\[
\frac{dV_C}{dt}_{\text{max}} = \frac{dV_{o1}}{dt}_{\text{max}}
\]  

(8.3)

8.4 Experimental validation

The circuit shown in Fig.8.5 was built and tested. \( A1 \) and \( A2 \) were 100 MHz bandwidth, single supply, rail to rail amplifiers, \( EL5444 \). \( D1, D2, D3 \) were fast Schottky diodes, \( BAT54 \). The storage capacitor: 1.2nF ceramic type. \( Q \) was n-channel MOSFET switch, \( BSS138 \). The storage time \( t_{st} = 3 \, \mu s \). The time delay \( t_d = 80 \, \text{ns} \). The input signal, \( V_{in} \), slew rate was \( 1V/63\text{ns} \). The peak detector did not work properly. Recorded results are shown in Fig.8.7. When the reset switch \( Q \) is off, a relatively steep input signal, \( V_{in} \), is applied to the positive input of \( A1 \). The output voltage of \( A1, V_{o1} \), goes to the positive saturation voltage after about 40 ns time delay. When \( V_{o} \) reaches \( V_{in}, A1 \) is still saturated. Returning to the linear operation mode takes about 30 to 40 ns. In this time \( C \) charges above \( V_{in} \), which is not desired.

Fig. 8.7: Peak detector waveforms – an example of a circuit not working properly (from Fig.8.5.)
8.5 Improved circuit

A modified circuit from Fig.8.5 is shown in Fig.8.8. New components have been added to obtain correct signal detection. Resistors: $R_I$, $R_4$ – set the gain of $A_I$ in linear operation region (important during small amplitude signal detection); $R_3$ – protects the output of $A_I$ when $Q_I$ is “on” and acts as charging current path during signal detecting time. Components $R_3$ and $C_2$ are a conditioning network acting at the beginning of a new peak detection. Diodes $D_4$ and $D_5$ are high-speed diodes ($BAV99W$). They act against positive saturation during steep high amplitude signal detection, see Fig.8.10 ($V_{ol}$ compare with Fig.8.7). Their combined forward voltage drop has to be higher than combined forward voltage drops of $D_1$ and $D_3$. Otherwise there is no charging current through $R_3$.

Fig. 8.8: Modified high frequency peak detector with reset.
Fig. 8.9: Peak detector equivalent circuits: a) during new peak detection, b) during holding time.

\( Q \) is n-channel MOSFET switch – BSS138. Circuit operates in two modes – detection and holding. Equivalent circuits are shown in Fig.8.9.

Modified peak detector works correctly. Example waveforms are shown in Fig.8.10. Associated time delay, \( t_d \), between \( V_{in} \) and \( V_o \) has to be taken into account during design process.
Fig. 8.10: Modified peak detector waveforms: a) The beginning of detection. b) One period of operation.

Output voltage, $V_o$, in a function of input voltage, $V_{in}$, and can be seen in Fig.8.11. The input voltage ranges from $0.35\text{V}$ to $2.25\text{V}$. Obtained accuracy is sufficiently good to use the peak detector in prototyping process.

![Graph of $V_o$ vs $V_{in}$](image)

Fig. 8.11: Output voltage of the peak detector as a function of input voltage: $V_o=f(V_{in})$. 
Nowadays a computer-aided analyse is an inherent part of the engineering design process. It allows us to explore unlimited "what if?" questions at the early stage of the design, before building a prototype. It is a very convenient design tool nevertheless, before it can be properly used, it is necessary to answer a few general questions.

- What are we going to simulate, a complete system or parts of it?
- What accuracy will satisfy us and what level of model complexity and the simulation time will we tolerate?
- What program is going to be used?
- What are the important results, especially in a complex systems?

We decided to verify our theoretical considerations on a novel control methodology for the flyback converters with simulation results. We were not planning highly accurate and detailed analysis of the circuit. We were looking for a rough and quick confirmation of our decisions at the early stage of the design process. In this situation a flyback converter with the complete control circuit (including a start-up circuit) had to be developed in the easiest possible way. As a simulation platform we decided to use (OrCAD) SPICE – *Simulation Program with Integrated Circuit Emphasis*. This widely available program has become the industry standard for computer-aided circuit analysis for microelectronic circuits [G13].

In this chapter we show the complete model of the converter and some simulation results, which have proven the correctness of our theoretical considerations.
9.1 Simulation model of flyback converter with cycle by cycle control circuit.

The complete schematic of the circuit consists of two pages, Fig.9.1 and Fig.9.2. The model is built with mixed digital and analogue components together with mathematical function blocks. Near to the components or groups of components some text labels are placed. The text labels correspond to a block diagram of the circuit shown in Fig.5.2, § 5.1.

Design specification was: $V_{in}=18$ to $22V$, $V_o=3V3$, $I_{o\max}=1A$, $f_s=250..500kHz$. Flyback transformer magnetising inductance is $30.44\mu H$, turns ratio is $11:4$. The input voltage, $V_{in}$, and the primary side switch voltage, $V_{sw}$, were divided by 20 ($Ko=1/20$), to be within the common mode input signals range of components used in the control circuit. The forward voltage drop of the output diode is measured directly, this idealised approach is to simplify the model.

The flyback converter is constructed with an input filter capacitor, $C_6=10\mu F$, a damping network, $R_{23}=37\Omega$ & $C_{343}=0.3nF$ and an output capacitor, $C_1=195\mu F$ & (esr) $R_{1196}=0.03\Omega$. The load resistance is $R_1$ with an option of parallel combination with $R_6$. The main switching MOSFET was an IRF640 device. As the output diode modified model of MBR1045 is used, parameter CJO was changed from $11.509E-9$ to $11.509E-15$. Another modified component in the model is an amplifier AD648. Its parameters: $c_1=11.66E-12$ and $c_2=25.00E-12$ were changed to $c_1=11.66E-15$ and $c_2=25.00E-15$. Modifications are done to speed-up these components. The rest of components used are standard from the library of SPICE.
Fig. 9.2: Second page of OrCAD schematic of a flyback converter with cycle by cycle control circuit.
9.2 Simulation results from the start-up circuit operation and the early stage of the voltage mode control

The start-up circuit is described in details in § 5.2. Here we show the main signals in the circuit. In Fig. 9.3 can be seen the output voltage, $V_o$, together with the reference voltage, $V_{ref}$ and in the upper screen two digital signals can be seen. $U118:Y$ is the output of logic1, this is the on-time. $N109129$ is the output signal $Q$ of constant off-time(2) – the constant off time during normal operation. These results are for $V_{in} = 18V$ and $R1 = 10\Omega$. In this case the output voltage reaches the reference level in about 520μs.

The beginning of the start-up process is shown in Fig. 9.4. It can be seen that the on-time is very short. The current limit is very low – the beginning of a ramp.

![Fig. 9.3: The output voltage during start-up, from 0V to 3V3, $V_{in} = 18V$, $R1 = 10\Omega$.]
Fig. 9.4: The output voltage during start-up, zoom of the first 80\(\mu\)s from Fig.9.3.

\(Q\) of constant off-time (2) is at logic low until the output voltage reaches certain level, output voltage threshold, see Fig.9.5. After that time the output voltage approaches \(V_{ref}\) under cycle by cycle voltage mode control.

Fig. 9.5: The first constant off-time when \(V_o\) is greater than Output voltage threshold, zoom of Fig.9.3.

The primary side current, \(I_p\), at time when \(V_o\) is greater than Output voltage threshold can be seen in Fig.9.6. The secondary side current at the same time can be seen in
Fig. 9.7. Observing these currents it can be seen that after cut-off the start-up circuit the energy transfer, as before, stays at the maximum level.

Fig. 9.6: The primary side current zoom around the time when $V_o > \text{Output voltage threshold}$ from Fig.9.5.

Fig. 9.7: The secondary side current zoom around the time when $V_o > \text{Output voltage threshold}$ from Fig.9.5.
Immediate limitation of transferred energy takes place when $V_o$ is bigger than $V_{ref}$. The output voltage crossing $V_{ref}$ can be seen in Fig.9.8. It can be seen that, in this case, the operation mode is changing from CCM to DCM, see Fig.9.9, $I_p$, and Fig.9.10, $I_s$.

![Graph showing voltage and current](image)

Fig. 9.8: Zoom of the moment when $V_o>V_{ref}$ from Fig.9.3.

![Graph showing current and time](image)

Fig. 9.9: The primary side current zoom around the time when $V_o>V_{ref}$ from Fig.9.8.
Fig. 9.10: The secondary side current zoom around the time when $V_o > V_{ref}$ from Fig. 9.8.

As an example for comparison with Fig. 9.3, we show the complete start-up process for different load conditions, $R_l = 5\Omega$, see Fig. 9.11. It can be seen that now $V_o$ reaches $V_{ref}$ in a longer time (~580μs) than for $R_l = 10\Omega$ (~500μs) which is normal in the case of current limitation.

Simulation results from the proposed powering-up circuit fully confirm the correctness of the initial assumptions and undertaken solutions.

Fig. 9.11: The output voltage during start-up, from 0V to 3V3, $V_{in} = 18V$, $R_l = 5\Omega$. 
9.3 Simulation results from the circuit operating under cycle by cycle voltage mode control

The simulated circuit starts up with the primary side current limited. When the powering-up process is ended the circuit operates under primary side cycle by cycle voltage mode control. This mode of control is switched on before $V_o$ reaches $V_{ref}$, §5.2. The control mode change is smooth and there is no overshoot when $V_o$ reaches $V_{ref}$, see Fig.9.12.

![Diagram of voltage transition](image)

Fig. 9.12: An example of complete powering-up process with transition into the normal operation mode, $R_1=10\Omega$, $V_{in}=18V$, $V_{ref}=3V3$.

A few cycles of the output voltage during the normal operation can be seen in Fig.9.13. It is for $R_1=10\Omega$, $V_{ref}=3V3$, $V_{in}=18V$. In Fig.9.13 it can be seen that there is no ideal operation point even for unchanged circuit conditions. Additionally there is no visible regular sequence in the output voltage ripples. The maximum spike is 3.3581V (+1.76% of $V_{ref}$) and the minimum spike is 3.2846V (-0.467% of $V_{ref}$). The primary side current and the secondary side current for the same conditions as in Fig.9.13 can be seen in Fig.9.14 and Fig.9.15 respectively.
Fig. 9.13: The output voltage during the normal operation, $R_l=10\Omega$, $V_{in}=18V$, $V_{ref}=3V3$.

Fig. 9.14: The primary side current during the normal operation, $R_l=10\Omega$, $V_{in}=18V$, $V_{ref}=3V3$. 
Fig. 9.15: The secondary side current during the normal operation, $R_l=10\Omega$, $V_{in}=18V$, $V_{ref}=3V3$.

The output voltage for changed load, $R_l=5\Omega$, $V_{in}=18V$, $V_{ref}=3V3$ is shown in Fig.9.16. The maximum spike is $3.3060V\ (+0.181\% \ of \ V_{ref})$ and the minimum spike is $3.2258V\ (-2.25\% \ of \ V_{ref})$. The primary and the secondary side currents can be seen in Fig.9.17 and Fig.9.18 respectively.

Fig. 9.16: The output voltage during the normal operation, $R_l=5\Omega$, $V_{in}=18V$, $V_{ref}=3V3$. 

Fig. 9.17: The primary side current during the normal operation, $R_1=5\Omega$, $V_{in}=18V$, $V_{ref}=3V3$.

Fig. 9.18: The secondary side current during the normal operation, $R_1=5\Omega$, $V_{in}=18V$, $V_{ref}=3V3$. 
The output voltage for a changed input voltage $V_{in}=22V$, $R_1=10\Omega$, $V_{\text{ref}}=3V3$ can be seen in Fig.9.19. The maximum spike is $3.3590V$ ($+1.788\%$ of $V_{\text{ref}}$) and the minimum spike is $3.2873V$ ($-0.384\%$ if $V_{\text{ref}}$). When compared with Fig.9.13 it can be noticed that for $22.222\%$ of the input voltage increase the maximum spike increased by $0.028\%$. The minimum spike decreased by $0.083\%$. The primary and the secondary side currents corresponding to Fig.9.19 are shown in Fig.9.20 and Fig.9.21 respectively. The simulated circuit provides static line and load regulation as expected.

![Graph showing the output voltage with maximum and minimum spikes labeled]

Fig. 9.19: The output voltage during the normal operation, $R_1=10\Omega$, $V_{in}=22V$, $V_{\text{ref}}=3V3$. 

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Fig. 9.20: The primary side current during the normal operation, $R_I=10\Omega$, $V_{in}=22V$, $V_{ref}=3V3$.

Fig. 9.21: The secondary side current during the normal operation, $R_I=10\Omega$, $V_{in}=22V$, $V_{ref}=3V3$. 
9.4 Simulation results from the dynamic line and load regulation

The developed model was also used to investigate dynamic behaviour of the flyback converter under primary side cycle by cycle control.

The load regulation example can be seen in Fig.9.22 and Fig.9.23. In Fig.9.22 can be seen the output voltage with the output current. The current changed from 32.7% to 63.79% in a repeatable sequence. The maximum output voltage, when the current was at 32.7% of \( I_{\text{omax}} \), was 3.3496V (+1.503% of \( V_{\text{ref}} \)). The minimum output voltage, when the current was at 63.79% of \( I_{\text{omax}} \), was 3.2294V (-2.139% of \( V_{\text{ref}} \)).

In Fig.9.23 can be seen the zoom of the output voltage and the output current together with the peak detector input and the output signals. During the simulation the peak detection area of the circuit caused the biggest problems with the convergence of the OrCAD simulator.

![Graph showing load regulation results](image)

**Fig. 9.22:** The output voltage and the output current during load regulation, when \( R_l \) changed from 10Ω to 5Ω, \( V_{in}=18V \), \( V_{ref}=3V3 \), \( V_{offset}=1V1 \).
Fig. 9.23: The output voltage and the output current together with the peak detector input and output signals during load regulation, when $R_1$ changed from 10Ω to 5Ω, $V_{in}=18V$, $V_{ref}=3V$, $V_{offset}=1V$.

The results for the input voltage changes can be seen in Fig.9.24 and Fig.9.25. In Fig.9.24 can be seen the input voltage change from 18V to 22V (full the design range) together with the output voltage and the output current. A better picture of the output voltage and the output current can be seen in Fig.9.25. The maximum output voltage is $3.3966V$ ($+2.927\%$ of $V_{ref}$), when in steady state operation, for the same circuit conditions, Fig.9.19, was $3.3590V$ ($+1.788\%$ of $V_{ref}$). The minimum output voltage is $3.2687V$ ($-0.948\%$ of $V_{ref}$) and is more than in the steady state operation, Fig.9.13, $3.2846V$ ($-0.467\%$ of $V_{ref}$).
Fig. 9.24: Line regulation, the input voltage changed from 18V to 22V, $R_1 = 10\Omega$, $V_{\text{ref}} = 3V$, $V_{\text{offset}(18V)} = 1V$, $V_{\text{offset}(22V)} = 1V35$.

Fig. 9.25: Line regulation, the output voltage and the output current, when the input voltage as in Fig.9.24 changed from 18V to 22V, $R_1 = 10\Omega$, $V_{\text{ref}} = 3V$, $V_{\text{offset}(18V)} = 1V$, $V_{\text{offset}(22V)} = 1V35$. 

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9.5 Summary of the simulation

The overall output voltage regulation was within the range of +/-3%. The simplified model of the peak detector limits the accuracy. Nevertheless, results obtained from the developed model have confirmed the correctness of assumptions made at the early stage of the design. At this stage we are ready to build the prototype.

When we compare the simulation results with the prototype results in Chapter 10, then it can be seen that the accuracy of the output diode model (directly measured in the simulation) has a strong influence on the overall regulation accuracy.
Chapter 10

Experimental results from the prototype

The theoretical considerations confirmed by mathematical symbolic equations analysis and good simulation results give a basis for development of rules and conditions for the circuit assemble. In this chapter we show results from the prototype circuit.

The first results from the prototype are shown in Appendix 2, where we analyse the flyback converter switch waveforms. These results are from the power path, which comprise: the input voltage; the input current; the switch voltage; the output voltage and signals across the output diode.

Firstly in this chapter are shown results from the control circuit and the natural limitations of the circuit due to the components used are discussed.

Next the static and the dynamic features of the prototype are investigated, including both line and load regulation performance.

10.1 The control path signals

The control mechanism proposed in this work is based on the output voltage calculated on the primary side, $\nu_{oc}$, of the converter in its off state, Eq. 3.9. An example of $\nu_{oc}$ can be seen in Fig. 10.1. The calculated output voltage is measured (at Pin 3 of U12) with a time delay, $t_d=660\text{ns}$, caused by delays of the components used. This time delay is measured between the switch voltage and the output signal of the peak detector. (Pin 14 of U36), see Fig. 10.2.

Fig. 10.3 and Fig. 10.4 are the same as Fig. 10.1 and Fig. 10.2 consequently, with measurement in the second cycle, when the output voltage is smaller. It can be seen that $\nu_{oc}$ is calculated precisely in each operation cycle. The oscilloscope cursor shows in Fig. 10.3 that $\nu_{oc}$ is $1.68\text{V}$, but the cursor’s cross is placed at the maximum value of the $\nu_{oc}$ trace, (in Fig. 10.1 the cross is at the minimum of the $\nu_{oc}$ trace). In this case it can be seen that $\nu_o$ in the second cycle is smaller than in the first cycle and as a consequence of
this, (\(v_{oc}\) is smaller too), in the second cycle the peak detector output signal is smaller, Fig.10.4.

**Fig. 10.1:** Half of the output voltage calculated during the off-time, \(v_{oc}=1.68V\) for \(v_o=3.38V\) (Fig.10.2), \(V_{in}=18V\).

**Fig. 10.2:** A time delay in the control circuit illustration, \(t_d=660ns\), and accurate measurement of the output voltage, \(v_o=3.38V\) (Ch4 with offset), \(V_{in}=18V\).
Fig. 10.3: Half of the output voltage calculated during the off-time, $v_{oc} = 1.675V$ for $v_o = 3.35V$ (Fig. 10.4), $V_{in} = 18V$.

A Gain&Phase analyser also measured the output voltage, over a range of frequency. See Fig. 10.5. It can be seen that the effective control loop frequency is about
4kHz. In this particular Gain&Phase test the gain rises up with the frequency which is not real, it is just a result of injecting the test signal into the input voltage. This measurement approach also shifts the phase by 180°. In this case, when we have used the Gain&Phase analyser in tests of the highly non-linear system, only the gain, at frequencies significantly lower from the switching frequency, \( f_s = 100..165kHz \), can be considered as the proper answer.

![Gain over Frequency and Phase over Frequency graphs](image)

Fig. 10.5: Gain and phase of \( V_{oc}/V_o \).

The regulation error can be seen in Fig.10.6 (Pin 8 of U12). It can be seen that for \( V_o = 3V3 \), the error signal is around zero.

![Regulation error graph](image)

Fig. 10.6: The regulation error example, \( V_o = 3V3 \).
Once we have the regulation error, after a gain \((U4)\) we add it to an offset voltage \((V_{\text{offset}}=1.24V\) for \(V_{\text{in}}=18V\)) and this is the input signal of the peak detector. In Fig.10.7 can be seen an example of the input signal of the peak detector \((\text{Pin 3 of } U36)\) and the output signal \((\text{Pin 14 of } U36)\).

![Input and Output Signal of Peak Detector](image)

Fig. 10.7: The peak detector input and the output signal.

The peak detector output signal is compared with a slope SG1 \((\text{Pin 3 of } U15)\) and the calculated on-time is obtained \((\text{Pin 5 of } U15)\), see Fig.10.8. The calculated on-time is reflected into the next operation cycle \((\text{Pin 5 of } U16)\) by the two slope technique using SG2 \((\text{Pin 3 of } U16)\) and SG3 \((\text{Pin 2 of } U16)\), see Fig.10.9.

![On-Time Calculation Example](image)

Fig. 10.8: The on-time calculation example, comparison at high signals level.
Fig. 10.9: The calculated on-time reflection into the next operation cycle.

In Fig. 10.8 can be seen that the comparison of $SGI$ and $PD_{output}$ is at a relatively high signal level, so the comparator responds immediately. In case of the $PD_{output}$ being at relatively low level, the comparator responds with some time delay, see Fig. 10.8 – second cycle (360ns). This is natural limitation of the component used and it sets the maximum calculated on-time in the prototype, (3.52μs), see Fig. 10.10.

Fig. 10.10: The maximum on-time calculation example, comparison at low signals level.
In Fig. 10.11 can be seen an example of the on-time variation during the control process. When we look at the switch voltage over a few operation cycles in Fig. 10.12, it can be seen that the steady state operation is achieved within two cycles (two cycles stability phenomena [G14]).

Fig. 10.11: The on-time variation during the control process.

Fig. 10.12: Transient behaviour over a few switching cycles, $V_{on}$.
10.2 Line and load regulation

The static line regulation curve is shown in Fig. 10.13. The characteristic was measured for $R_{\text{load}}=5.6\Omega$ and $V_{\text{ref}}=3V3$. It can be seen that in the range of $V_{\text{in}}=15..19V$ the average output voltage changes from $V_o=3.241..3.321V$. This gives a line regulation accuracy of $-1.787\%$ to $+0.636\%$. The offset voltage was set manually according to Eq. 5.14.

![Static line regulation curve](image)

Fig. 10.13: Static line regulation curve, $R_{\text{load}}=5.6\Omega$ and $V_{\text{ref}}=3V3$.

The static load regulation curve is shown in Fig. 10.14. The characteristic was measured for the nominal input voltage, $V_{\text{in}}=18V$ and $V_{\text{ref}}=3V3$. The offset voltage, $V_{\text{offset}}=1.24V$.

![Static load regulation curve](image)

Fig. 10.14: Static load regulation curve, $V_{\text{in}}=18V$ and $V_{\text{ref}}=3V3$, $V_{\text{offset}}=1.24V$, the error gain, $K2=10$. 

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In the prototype, the simplified model of the output diode seriously reduced the accuracy of the static regulation. Additionally in the static load regulation curve can be seen a bump, which is caused by limiting diodes, \( CR3 \) and \( CR4 \). The presence of this limiting network is dictated by the common mode input signals range of the components used. It is highly advisable to use more integrated circuits in future tests.

Dynamic load regulation waveforms for the load current change from 0.35A to 0.85A are shown in Fig.10.15. It can be seen that the output voltage jumps from one operation point to another one, according to the static load regulation curve, Fig.10.14. There is no overshoot or oscillations and it can be seen that the gain, \( K2=10 \), could be higher to eliminate the slow approach to the operation point after the main transient slope. In Fig.10.16 and Fig.10.17 can be seen a zoom of the transient behaviour from Fig.10.15, rising and decaying slopes. The rising transient time is about \( 300\mu s (~35 \text{ cycles}) \) and the falling about \( 200\mu s (~25 \text{ cycles}) \), respectively.

![Graph showing load change from 0.35A to 0.85A, with \( V_{in}=18V \), \( Ch2-V_o \), \( Ch4-I_o \), \( K2=10 \).](image)

**Fig. 10.15:** Load change from 0.35A to 0.85A, \( V_{in}=18V \), \( Ch2-V_o \), \( Ch4-I_o \), \( K2=10 \).
Fig. 10.16: $V_o$ rising slope and $I_o$ from Fig.10.15.

Fig. 10.17: $V_o$ decaying slope and $I_o$ from Fig.10.15.
In Fig. 10.18 results for changed input voltage can be seen, $V_{in}=16\,\text{V}$ and $V_{offset}=1.02\,\text{V}$. The output current is changing from 0.45A to 0.6A. It can be seen that as in Fig.10.15, the operation point is changing, but in a narrower range, according to a static characteristic. The transient times for the rising, Fig.10.19, and falling, Fig.10.20, slopes are also shorter when compared with the previous results.

![Graph](image)

Fig. 10.18: Load change from 0.45A to 0.6A, $V_{in}=16\,\text{V}$, $Ch2-V_o$, $Ch4-I_o$, $K2=10$.

![Graph](image)

Fig. 10.19: $V_o$ rising slope and $I_o$ from Fig.10.18.
Fig. 10.20: $V_o$ decaying slope and $I_o$ from Fig.10.18.

For comparison with results shown in Fig.10.15 to Fig.10.17, $K_2=10$, we show in Fig.10.21 to Fig.10.23 results with the error gain, $K_2=33$. The input and the output circuit conditions are the same, $V_{in}=18$V, the output current is changing from 0.35A to 0.85A.

Fig. 10.21: Load change from 0.35A to 0.85A, $V_{in}=18$V; $Ch2-V_o$, $Ch4-I_o$. The gain=33
It can be seen in Fig. 10.22, that the rising time is now shorter, about 250µs instead of 300µs, and there is no slow approach when the voltage is getting closer to the upper level. The falling time, Fig. 10.23 is about 150µs instead of 200µs. And there are no overshoot or transient oscillations.

Fig. 10.22: $V_o$ rising slope and $I_o$ from Fig. 10.21.

Fig. 10.23: $V_o$ decaying slope and $I_o$ from Fig. 10.21.
10.3 Summary

Results obtained from the prototype prove that the original concepts from the theoretical considerations and simulation analysis of the proposed control mechanism for isolated flyback converters are correct. Nevertheless, limited regulation accuracy over the full range of the operation of the prototype gives us encouragement for future work and improvement of this novel control technique. The first step for better accuracy is an integrated solution, which will eliminate significant parasitic components from the signal-processing path. And perhaps a better place for this control mechanism would be on the secondary side of the converter, where the voltage across the output diode or a SR MOSFET can be measured directly. But this approach will introduce another interesting challenge, namely the line regulation.
Chapter 11

Conclusion and Recommendation for Future Work

The thesis has achieved what it has set out to do – namely to develop a method by which a flyback DC/DC converter may be accurately controlled using a novel primary-side control mechanism that dispenses with the need for the traditional isolation component between the secondary and primary elements of the control loop. This will have several advantages for commercial DC/DC converter development:

- Fewer components allow higher power density in converters (reduced board area for components).
- Fewer components mean longer MTBF for the converter.

The removal of the isolation barrier from secondary to primary eliminates the disadvantages associated with traditional methods. These are listed below, along with their major disadvantages:

**Opto-coupler isolation**

- Degradation of optocoupler CTR over lifetime is a major issue in traditional feedback loops. This circuit eliminates this component and allows easier, more accurate design of the control loop with better performance over the product lifetime.
- The maximum operating temperature of optocouplers is 105°C and this is much lower than that for other components such as resistors, capacitors, MOSFETS. Elimination of this component allows the converter operate in a hotter environment or at increased power – both important considerations in today’s marketplace.

**Magnetic isolation**

- Signal transformers add complexity to the system and are unsuitable in many applications.

**Capacitive isolation**

- This is also unpopular due to cost issues involved in ensuring safety standards are met.
The particular achievements of this thesis are:

- The traditional isolation between primary and secondary has been eliminated from the control loop.

- An isolated DC/DC converter without feedback from the load was demonstrated
  - Control is primary-side only and uses the switch voltage and the input voltage along with an innovative control topology.
  - The converter operated at constant off-time and variable on-time for both continuous and discontinuous conduction modes.
  - The input voltage range of the converter is 16-24Vdc and delivers 3.3V, 1.2A at a variable switching frequency in the range 100-165kHz.

- Detailed analyses of this converter were presented, including:
  - Accurate mathematical modeling of the converter, including all important parasitics.
  - Comprehensive OrCAD model was developed to accurately simulate the circuit performance over a variety of external stimuli (see Chapter 9).
  - The mathematical model and simulation were both verified by the prototype model.
  - This model was further developed into schematics of converters utilising the following switching mechanisms (flyback converters):
    - Constant on-time, variable off-time (see Chapter 6, Section 6.3).
    - Variable off-time, variable on-time, variable frequency (see Chapter 6, Section 6.4).
    - Constant Switching frequency (see Chapter 6, Section 6.5).

A working model, both theoretical and physical was produced for converters operating with a constant off-time, variable on-time. The theoretical models were strongly based upon empirical measurement on the prototype converter to provide a solution that most accurately reflected real circuit operation. This proven model was extended theoretically to show how the flyback converters with other switching mechanisms could be controlled using this novel control methodology.
However there are many possibilities of extending the research undertaken in this thesis. The following list suggests some areas of research to further the developments in this project:

- In order to commercially realise this topology it should be implemented in an integrated circuit. This should be the next stage of the project. This will help reduce component count in the converter, reduce cost and allow better control over parasitic elements in the loop.
- Investigate implementing a secondary side solution as an alternative to this primary-side controller. This allows direct access to the forward voltage drop of the output diode. However, this approach will introduce another interesting challenge, namely the line regulation (how to transmit input voltage information across the isolation barrier).
- Implement the topology using a synchronous rectifier at the output rather than a Schottky diode. This would allow more accurate output voltage calculation as the non-linear characteristic of the diode is replaced by linear characteristic of the SR MOSFET.
- Investigate the following theoretical models in a physical circuit:
  - Constant off-time, variable on-time with single-slope implementation and reset (a) at the end of the on-cycle and (b) at the beginning of the off-time.
  - Constant on-time, variable off-time.
  - Variable on-time, variable off-time, variable frequency.
  - Constant switching frequency.
REFERENCES

FLYBACK CONVERTER


Modelling


**CONTROL**


**MAGNETICS**


**GENERAL**


AUTHORS PUBLICATIONS


BOOKS


[G7] Private correspondence with Mr. Peter Bardos, Principal Engineer in Artesyn Technologies, Youghal, Ireland.


**WORK HANDBOOKS**

[H1] TDK’s EPC cores.
Note that in the indexes of equations below the first part, A1, indicates the appendix number. The second part of the indexes is the chapter number where the equation is discussed (should be placed). And the third part of the indexes is the equation number.

\[
\text{(A1.2.21)}
\]

\[
Y = \left(\sqrt{\frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}}} - \frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}} \right) + \frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}}
\]

\[
\sin \left(\frac{1}{2} \sqrt{\frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}}} \right) \cos \left(\frac{1}{2} \sqrt{\frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}}} \right)
\]

\[
\exp \left(\frac{1}{2} \sqrt{\frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}}} \right)
\]

\[
\exp \left(\frac{1}{2} \sqrt{\frac{-2 L_s R C \exp - 4 L_s R^2 C + \exp^2 C^2 R^2 + L_s L}{{L_s^2 C^2 (\exp + R)^2}}} \right)
\]
\[
\text{ioff} = \left( \begin{array}{c}
-R^2 C^2 + 2 R C^2 \sqrt{-2 L R C \text{esr} - 4 L R^2 C + \text{esr}^2 C^2 R^2 + L s^2} \\
\frac{L s^2 C^2 (R + s)^2}{L s^2 C^2 (R + s)^2}
\end{array} \right)
\]
\[
V_{\text{DCM0}} := -\frac{1}{2} \arctan \left( \frac{1}{2} \frac{\text{Isqff0} \left( -2 R T^2 \text{esr} - 4 R^2 T^2 + Ls^2 \right)}{T^2 \left( R + \text{esr} \right)} \right)
\]

\[
\left( R \text{Isqff0} C \text{Vcoff0 esr} + \text{Isqff0}^2 R Ls + C R \text{Vcoff0}^2 - \text{Ls Isqff0 Vcoff0} \right) \left( R \text{Isqff0} C \text{esr} + \text{Ls Isqff0} - 2 C R \text{Vcoff0} \right) \left( \frac{C R \left( R \text{Isqff0} C \text{Vcoff0 esr} + \text{Isqff0}^2 R Ls + C R \text{Vcoff0}^2 - \text{Ls Isqff0 Vcoff0} \right)}{\left( -R \text{Isqff0} C \text{esr} + \text{Ls Isqff0} - 2 C R \text{Vcoff0} \right)^2} \right) ^{\frac{1}{2}}
\]

\[
\begin{align*}
\text{God} & := \left( (2 \text{esr}^2 D1 Lm R Co + \text{esr D1} Lm R^2 Co + \text{esr}^3 D1 Lm Co) s^2 + (TR^2 R^3 \text{esr Co D1}^2 + TR^2 R \text{esr}^3 Co - 2 TR^2 R \text{esr}^3 Co D1 \right) \\
& - 4 TR^2 R^2 \text{esr}^2 Co D1 + 2 R Lm \text{esr} D1 + \text{esr}^2 D1 Lm \\
& + 2 TR^2 R^2 \text{esr}^2 Co D1^2 + 2 TR^2 R^2 \text{esr}^2 Co + TR^2 R \text{esr}^3 Co D1^2 \\
& + Lm R^2 D1 - 2 TR^2 R^3 \text{esr Co D1} + TR^2 R^3 \text{esr Co}) s + 2 TR^2 R^2 \text{esr} D1^2 \\
& + TR^2 R^3 D1^2 - 2 TR^2 R \text{esr}^2 D1 - 4 TR^2 R^2 \text{esr} D1 + TR^2 R \text{esr}^2 \\
& + TR^2 R \text{esr}^2 D1^2 + TR^2 R^3 + 2 TR^2 R^2 \text{esr} - 2 TR^2 R^3 D1) \text{Vin} \right) \left( (Lm R^2 Co + 2 Lm R Co \text{esr} + Lm \text{esr}^2 Co) s^2 + (TR^2 R \text{esr}^2 Co \\
& + TR^2 R^2 \text{esr Co} - TR^2 R \text{esr}^2 D1 Co - 2 Lm \text{esr} D1 + Lm \text{esr} \\
& - TR^2 R^2 \text{esr D1 Co} + Lm R - 2 Lm R D1) s + 2 TR^2 R \text{esr} D1^2 + TR^2 R^2 \\
& - 2 TR^2 R^2 D1 + TR^2 R^2 D1^2 - 3 TR^2 R \text{esr} D1 + TR^2 R \text{esr} \right) \\
& (2 \text{esr} D1 - \text{esr} - R + R D1) (-1 + D1) TR) \\
\end{align*}
\]

\[
\begin{align*}
\text{God} & := \sqrt{2} \left( \sqrt{\frac{Lm}{TR^2 Ts R}} R TR ((\text{esr} C R + C \text{esr}^2) s + R + \text{esr}) Vin Ts \\
& \left( (Lm C Ts \text{esr}^2 + Lm C Ts R^2 + 2 Lm C Ts R \text{esr}) s^2 + (Ts Lm \text{esr} \\
& + Ts \sqrt{2} \left( \sqrt{\frac{Lm}{TR^2 Ts R}} R TR^2 \text{esr}^2 C + Ts Lm R \\
& + Ts \sqrt{2} \left( \sqrt{\frac{Lm}{TR^2 Ts R}} R^2 TR^2 \text{esr} C \right) s + 2 Lm R \\
& + \sqrt{2} \left( \sqrt{\frac{Lm}{TR^2 Ts R}} R TR^2 \text{esr} Ts \right) \right) \right)
\end{align*}
\]
\[ C_{sum} := (16 \text{ } Lm \text{ } \pi \text{ } f \text{ } CDS^2 \text{ } Rpd^2 \text{ } Cpd^2 + 4 \text{ } Lm \text{ } \pi \text{ } f \text{ } CDS^2 + 4 \text{ } Lm \text{ } Rpd^2 \text{ } \pi \text{ } f \text{ } Cpd^2 + Lm \\
- 4 \text{ } CDS \text{ } Rp_{tr}^2 \text{ } Rpd^2 \text{ } \pi \text{ } f \text{ } Cpd^2 - CDS \text{ } Rp_{tr}^2 - 16 \text{ } CDS \text{ } \pi \text{ } f \text{ } Lm^2 \text{ } Rpd^2 \text{ } Cpd^2 - 4 \text{ } CDS \text{ } \pi \text{ } f \text{ } Lm^2 \\
- 4 \text{ } Cpd \text{ } Rp_{tr}^2 \text{ } \pi \text{ } f \text{ } CDS^2 + Cpd \text{ } Rp_{tr}^2 - 16 \text{ } Cpd \text{ } \pi \text{ } f \text{ } Lm^2 \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{ } \text{
APPENDIX 2

Note that the first part, A2, of the figure numbers indicates the appendix number. The second part of the numbers is a chapter number where the figure is considered. And the third part of the numbers is the figure number.

Experimental results

For chosen input voltage $V_{in}=18V$ and $V_o=3.3V$ values of the output and the input capacitors were changed. Tests were done for the output currents $I_o=0.62A$ and $I_o=0.4A$. The converter was operating in DCM – the worst case test conditions.

Experiment 2

Fig.A2.3.9 to Fig.A2.3.12 are for $I_o=0.62A$ The input capacitance is $C_{in}=1\mu F$ and the output capacitance is $C_o=10\mu F$ ceramic cap. plus $1*6800\mu F$ electrolytic cap. The input voltage is shown in Fig.A2.3.9a – there is no significant change comparing with Fig.3.5a. Change can be seen in the output voltage, Fig.A2.3.9b. The oscillation’s frequency is higher compared with Fig.3.5b. Amplitudes are also different.

Fig. A2.3.9: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F$, $C_o=10\mu F+1*6800\mu F$: a) $v_{in}$, b) $v_o$. 
The switch voltage, Fig.A2.3.10, as in the previous case is constructed respectively to Eq.3.1.

\[ V_{\text{in}} = 18\, \text{V}, \quad V_o = 3.3\, \text{V}, \quad I_o = 0.62\, \text{A}, \quad C_{\text{in}} = 1\, \mu\text{F}, \quad C_o = 10\, \mu\text{F} + 1 \times 6800\, \mu\text{F} \]

Fig. A2.3.10: a) zoom of \( v_{\text{SW}} \), b) zoom of \( v_{\text{SW}} \).

The switch current, Fig.A2.3.11, is equivalent to Fig.3.7 and can be analysed and explained in the same way.
Fig. A2.3.11: $V_{in}=18\text{V}$, $V_o=3.3\text{V}$, $I_o=0.62\text{A}$, $C_{in}=1\mu\text{F}$, $C_o=10\mu\text{F}+1*6800\mu\text{F}$: a) $i_{sw}$ complete, b) zoom of $i_{sw}$ around zero level, c) zoom of $i_{sw}$ at the beginning of the off-time.

The forward voltage drop of the output diode can be seen in Fig.A2.3.12. It is also equivalent to Fig.3.8 and can be explained in the same way.
Fig. A2.3.12: $V_{in}=18\text{V}$, $V_o=3.3\text{V}$, $I_o=0.62\text{A}$, $C_{in}=1\mu\text{F}$, $C_o=10\mu\text{F}+1*6800\mu\text{F}$: a) $v_F$ of the output diode complete, b) zoom of the slope of $v_F$, c) zoom of the beginning of $v_F$.

Experiment 3

Fig. A2.3.13 to Fig. A2.3.15 are for $I_o=0.62\text{A}$ The input capacitance is $C_{in}=1\mu\text{F}$ and the output capacitance is $C_o=10\mu\text{F}$ ceramic cap. plus $2*6800\mu\text{F}$ electrolytic cap. Results are presented in the same form as before. The zoom of the initial current ripple and the forward voltage drop of the output diode are not shown.

The input voltage is shown in Fig. A2.3.13a – there is no significant change comparing with Fig. 3.5a and Fig. A2.3.9a. Change can be seen in the output voltage, Fig. A2.3.13b. The oscillation’s frequency is higher comparing with Fig. 3.5b and Fig. A2.3.9b. The output voltage oscillation is less damped. Amplitudes are also different.
The switch voltage can be seen in Fig. A2.3.14. It can be seen that the input voltage shape, $v_{in}$, dominates in $v_{sw}$, once the amplitude of $v_o$ is getting smaller.

The switch current can be seen in Fig. A2.3.15. It is without significant change.
Fig. A2.3.15: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F$, $C_o=10\mu F+2\times6800\mu F$: a) $i_{sw}$ complete, b) zoom of $i_{sw}$ around zero level.

Experiment 4

Fig.A2.3.16 to Fig.A2.3.19 are for $I_o=0.62A$. The input capacitance is $C_{in}=1\mu F$ (film cap.) plus $820\mu F$ (electrolytic cap.) and the output capacitance is $C_o=10\mu F$ ceramic cap. plus $100\mu F$ tantalum cap. Results are presented in the same form as for Fig.3.5 to Fig.3.8.

The input voltage can be seen in Fig.A2.3.16a. Comparing with Fig.3.5a, Fig.A2.3.9a, Fig.A2.3.13a big differences can be seen. Now some oscillations ($1MHz$) can be seen and the amplitude is significantly smaller than before. The output voltage, Fig.A2.3.16b, looks the same as in Fig.3.5b.
The input voltage oscillation from Fig.A2.3.16a can be seen in the switch voltage shown in Fig.A2.3.17 – this additionally confirms the correctness of Eq.3.1.

The switch current is shown in Fig.A2.3.18. There is no significant change comparing with Fig.3.7, Fig.A2.3.11 and Fig.A2.3.15.
Fig. A2.3.18: $V_{in}=18\,V$, $V_o=3.3\,V$, $I_o=0.62\,A$, $C_{in}=1\mu F+820\mu F$, $C_o=10\mu F+100\mu F$: a) $i_{sw}$ complete, b) zoom of $i_{sw}$ around zero level, c) zoom of $i_{sw}$ at the beginning of the off-time.

Forward voltage drop of the output diode can be seen in Fig.A2.3.19. It is the same as in Fig.3.8 and Fig.A2.3.12.
Fig. A2.3.19: $V_{in} = 18V$, $V_o = 3.3V$, $I_o = 0.62A$, $C_{in} = 1\mu F + 820\mu F$, $C_o = 10\mu F + 100\mu F$: a) $v_F$ of the output diode - complete, b) zoom of the slope of $v_F$, c) zoom of the beginning of $v_F$.

Experiment 5

Fig. A2.3.20 to Fig. A2.3.23 are for $I_o = 0.62A$. The input capacitance is $C_{in} = 1\mu F$ (film cap.) plus $820\mu F$ (electrolytic cap.) and the output capacitance is $C_o = 10\mu F$ ceramic cap. plus $1*6800\mu F$ electrolytic cap. Results are presented in the same form as for Fig. A2.3.9 to Fig. A2.3.12.
The input voltage, Fig.A2.3.20a, is the same as in Fig.A2.3.16a. The output voltage, Fig.A2.3.20b, is the same as shown in Fig.A2.3.9b. The switch voltage, $v_{sw}$, shown in Fig.A2.3.21 is as expected too.

**Fig. A2.3.20:** $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F+820\mu F$, $C_o=10\mu F+1*6800\mu F$: a) $V_{in}$, b) $V_o$.

**Fig. A2.3.21:** $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F+820\mu F$, $C_o=10\mu F+1*6800\mu F$: a) $v_{sw}$, b) zoom of $v_{sw}$.

The switch current, $i_{sw}$, waveform shown in Fig.A2.3.22 and the forward voltage drop, $V_f$, of the output diode, Fig.A2.3.23 are also without visible changes when compared with Fig.A2.3.11 and Fig.A2.3.12 respectively.
Fig. A2.3.22: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F+820\mu F$, $C_o=10\mu F+1*6800\mu F$: a) $i_{sw}$ complete, b) zoom of $i_{sw}$ around zero level, c) zoom of $i_{sw}$ at the beginning of the off-time.
Fig. A2.3.23: $V_{in}=18\text{V}$, $V_o=3.3\text{V}$, $I_o=0.62\text{A}$, $C_{in}=1\mu\text{F}+820\mu\text{F}$, $C_o=10\mu\text{F}+1*6800\mu\text{F}$: a) $v_F$ of the output diode - complete, b) zoom of the slope of $v_F$, c) zoom of the beginning of $v_F$.

Experiment 6

Fig. A2.3.24 to Fig. A2.3.26 are for $I_o=0.62\text{A}$ The input capacitance is $C_{in}=1\mu\text{F}$ (film cap.) plus $820\mu\text{F}$ (electrolytic cap.) and the output capacitance is $C_o=10\mu\text{F}$ ceramic cap. plus $2*6800\mu\text{F}$ electrolytic cap. Results are presented in the same form as for Fig. A2.3.13 to Fig. A2.3.15.
The input voltage, Fig.A2.3.24a, is the same as in Fig.A2.3.16a and Fig.A2.3.20a. The output voltage, Fig.A2.3.24b, is the same as shown in Fig.A2.3.13b.

Fig. A2.3.24: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F+820\mu F$, $C_o=10\mu F+2*6800\mu F$: a) $v_{in}$, b) $v_o$.

The switch voltage complete waveform, Fig.A2.3.25a, and zoom, Fig.A2.3.25b, contains oscillations of $v_{in}$ and $v_o$.

Fig. A2.3.25: $V_{in}=18V$, $V_o=3.3V$, $I_o=0.62A$, $C_{in}=1\mu F+820\mu F$, $C_o=10\mu F+2*6800\mu F$: a) $v_{sw}$, b) zoom of $v_{sw}$. 
The switch current can be seen in Fig.A2.3.26, and it behaves in the same way as in previous experiments.

Experiment 7

We have also changed the output current from $I_o=0.62$A to $I_o=0.4$A. Results can be seen in Fig.A2.3.27a, $v_{in}$, and Fig.A2.3.27b, $v_o$. The input capacitance is $C_{in}=1\mu$F (film cap.) plus 820uF electrolytic cap. and the output capacitance is $C_o=10\mu$F ceramic cap. plus 100uF tantalum cap. When these results are compared with Fig.A2.3.16a and Fig.A2.3.16b respectively then we can see that there is a change in signal amplitude, but not in frequency. Obviously DCM starts earlier for smaller output current. The same effect is for different capacitances – only the amplitude changes.
Fig. A2.3.27: $V_{in}=18\,\text{V}, \quad V_o=3.3\,\text{V}, \quad I_o=0.4\,\text{A}, \quad C_{in}=1\mu\text{F}+820\mu\text{F}, \quad C_o=10\mu\text{F}+100\mu\text{F}$: a) $v_{in}$, b) $v_o$. 
APPENDIX 3

The final prototype circuit

Fig. A3: A Picture of the final prototype circuit.
ALL HOLE SIZES ARE FINISHED SIZES
ALL ARTWORKS ARE VIEWED FROM THE COMPONENT SIDE

1. MANUFACTURED IN ACCORDANCE WITH ARTESYN
   SPECIFICATION NO. 330030-01.
   NOTED: UNLESS OTHERWISE SPECIFIED

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ALL DRAWINGS VIEWED FROM THE TOP SIDE
APPENDIX 4

The primary side output voltage calculation with an external peak detector circuit.

Fig. A4: Experimental circuits: bigger – the output voltage calculation on the primary side; smaller – a peak detector circuit.
APPENDIX 5

The first circuit.

Fig. A5: The first trial circuit.