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Low-loss, compact, spot-size-converter based vertical couplers for photonic integrated circuits

Praveen K.J. Singaravelu
Centre for Advanced Photonics & Process Analysis, Cork Institute of Technology, Cork, Ireland; Tyndall National Institute, Cork, Ireland, Praveen.Singaravelu@tyndall.ie

G.C.R. Devarapu
Centre for Advanced Photonics & Process Analysis, Cork Institute of Technology, Cork, Ireland,Tyndall National Institute, Cork, Ireland; Scottish Universities Physics Alliance, School of Physics & Astronomy, St Andrews, UK, Chinna.Devarapu@cit.ie

Sebastian A. Schulz
Centre for Advanced Photonics & Process Analysis, Cork Institute of Technology, Cork, Ireland; Scottish Universities Physics Alliance, School of Physics & Astronomy, St Andrews, UK

Quentin Wilmart
University Grenoble Alpes, CEA, LETI, MINATEC Campus, CEA-Grenoble, Grenoble, F38054, France

Stéphane Malhouitre
University Grenoble Alpes, CEA, LETI, MINATEC Campus, CEA-Grenoble, Grenoble, F38054, France.

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P.K.J. Singaravelu[1, 3], G.C.R. Devarapu[1, 2, 3], Sebastian A. Schulz[1, 2], Quentin Wilmart[4], Stéphane Malhouitre[4], Ségolène Olivier[4] and L. O 'Faolain[1, 2, 3]

[1] Centre for Advanced Photonics & Process Analysis, Cork Institute of Technology, Cork, Ireland.
[2] Scottish Universities Physics Alliance, School of Physics & Astronomy, St Andrews, UK.
[3] Tyndall National Institute, Cork, Ireland.
[4] University Grenoble Alpes, CEA, LETI, MINATEC Campus, CEA-Grenoble, Grenoble, F38054, France.

E-mail: praveen.singaravelu@my.cit.ie

Abstract

In recent years, the monolithic integration of new materials such as SiN, Ge and $LiNbO_3$ on silicon (Si) has become important to the Si photonics community due to the possibility of combining the advantages of both material systems. However, efficient coupling between the two different layers is challenging. In this work, we present a spot size converter based on a two-tier taper structure to couple the optical mode adiabatically between Si and SiN. The fabricated devices show a coupling loss as low as 0.058 dB ± 0.01 dB per transition at 1525 nm. The low coupling loss between the Si to SiN, and vice versa, reveals that this interlayer transition occurs adiabatically for short taper lengths (<200 μm). The high refractive index contrast between the Si and SiN is overcome by matching the optical impedance. The proposed two-tier taper structure provides a new platform for optoelectronic integration and a route towards 3D photonic integrated circuits.

Keywords: spot size converters, two-tier tapers and vertical coupling

1. Introduction

Low cost, low power consumption and high-speed optical interconnects are crucial components required to address the bandwidth bottleneck in datacentres that arises from the exponential growth of internet use [1]. Silicon photonics offers a high bandwidth, low-power consumption and a cost-effective approach through its compatibility with the standard Complementary Metal Oxide Semiconductor (CMOS) fabrication process [2]. The silicon-on-insulator (SOI) platform is widely used in silicon photonics because it allows the realization of both high-performance optoelectronic components, e.g. high-speed modulators and photodetectors [3,4] and passive elements, such as low-loss waveguides or high-quality optical resonators [5,6]. Together with efficient coupling schemes, such as grating couplers and spot size converters [7,8] for fibre-to-chip coupling, the SOI platform provides many of the vital elements required for on-chip, inter-chip and optical communications links.

The high refractive index of Si (n_{Si}=3.475 at 1550nm), provides tight confinement of the optical mode inside waveguides of widths as low as 400 nm. However, due to the high refractive index of Si, even small fabrication imperfections will negatively affect the optical mode's propagation in the waveguide, creating phase errors. Furthermore, the high thermo-optic coefficient (TOC) of Si (α_{Si}=1.8 X 10^{-4} K^{-1}) makes optical resonators, such as ring resonators, very sensitive to the temperature fluctuations (for some devices, a 10°C increase in the ambient temperature shifts resonances wavelength by 0.8nm) [9]. Therefore, the co-integration of new materials with low refractive index and

small thermo-optic coefficient is needed to improve the usefulness of the overall photonic integrated circuits.

1.1 SiN integration on SOI

Silicon nitride (SiN) is a CMOS compatible material and has long been utilised in the fabrication of electronics components. Silicon Nitride also is a powerful material for photonics application. For example, silicon nitride allows the fabrication of low-loss array-waveguide gratings (AWGs) for wavelength-division multiplexing (WDM) [10]. Moreover, due to the low refractive index (n_{SiN}=1.875 at 1550nm) and low TOC (α_{SiN}=1.7 X 10^{-5} K^{-1}) [16], SiN is more suitable than silicon for wavelength-selective elements such as gratings [11], ring-resonators [12] and photonic crystals [13], for example as mirrors in hybrid laser technology [11]. However, the direct co-planar integration of SiN with silicon waveguides limits the pattern density and scalability. This can be overcome by the vertical integration of SiN with Si, providing an extra dimension for the design of photonic components [4]. However, such vertical integration raises the important question of coupling the light efficiently between the two layers.

In the case of butt coupling, the coupling efficiency between the optical modes of the Si and SiN waveguides is low, due to the high refractive index contrast that results in Fresnel reflection. To achieve the maximum coupling efficiency, tapers should be introduced and the optical impedance matching condition must be satisfied as described in ref [14]:

i. The taper length should be long enough to couple the optical mode adibatically.
ii. The taper width should be chosen such that the effective refractive index discontinuity between the two layers is minimised to decrease the reflection loss and thus maximise the coupling efficiency.

In our vertical coupling scheme, this impedance matching is achived by tapering the width of the Si strip waveguide, resulting in tapers with different tapering schemes such as linear or exponential geometries [16]. In all of these tapers where only one geometric parameter is optimised (i.e. width of the waveguide), the effective coupling usually occurs at long taper lengths due to the slow adiabatic evolution of the optical mode from Si to SiN and vice-versa. Thus, these strip waveguide tapers result in large device footprints, placing a limit on the achievable device density and negating the advantage of vertical coupling.

To overcome this limitation, we propose a two-tier Si taper geometery [17], as shown schemtically in Fig 1 (a). This design allows independent control of the two sections of the Si taper waveguide and provides a fast adibatic coupling of the mode. The proposed SSC consists of a SiN waveguide vertically integrated above a Si tapered waveguide and seperated by a SiO_2 spacing layer. The silicon waveguide is tapered in two steps, first the top half, followed by the bottom half as shown in Fig 1 a. This ensures an adiabatic transition while reducing the device length. The SiN waveguide was used to couple the light in and out. To ensure the light couples into the Si layer, the SiN waveguide was not continuous in the middle of the chip. We used one coupler to couple the light into the Si layer and another coupler (rotated by 180 degrees) to couple it back into the SiN waveguide.

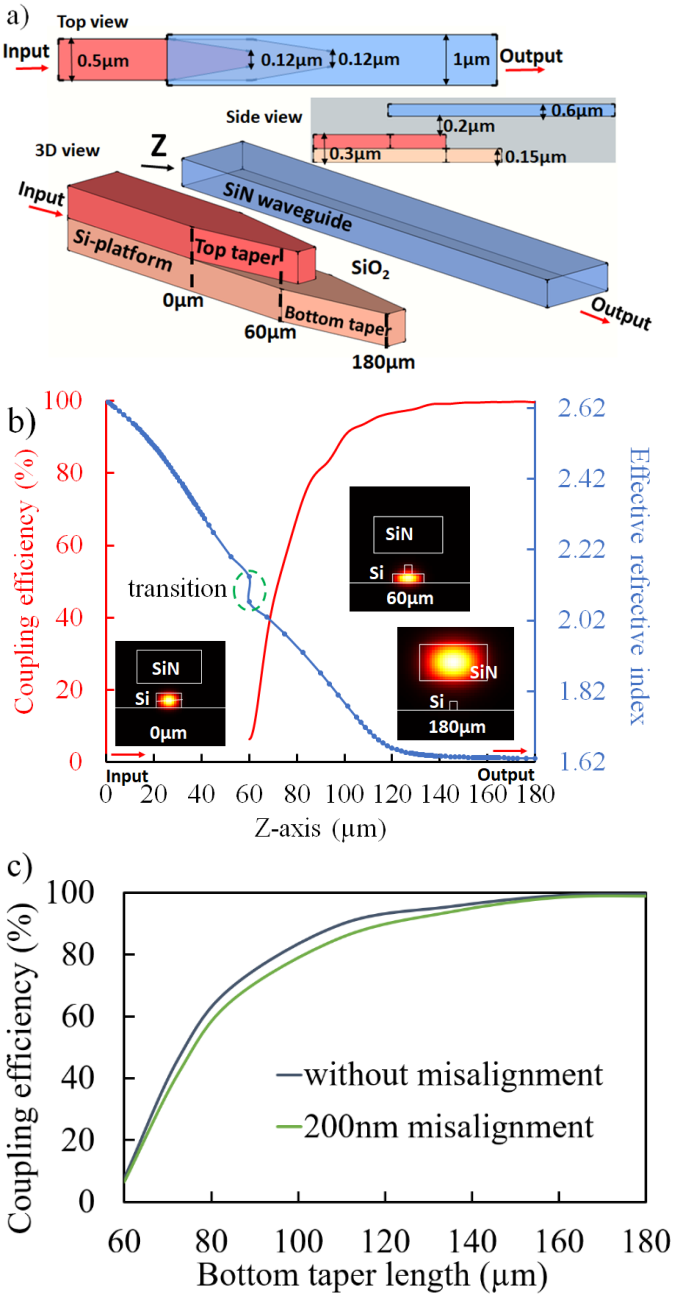


Figure 1: a) Schematic of the vertical integrated Si spot size converter with SiN wavegide, separated by a SiO_2 layer. input and ouput arrows indicate the light propagation direction (i.e. *Z*-axis), inset top view and side view. b) The solid red line shows the simulated coupling efficiency of the schematic design and the effective refractive index of the propagating

mode (TE) is indicated by solid blue line. The green dashed circle represents the mode transition from top to bottom taper. The mode profiles at 0 µm (input - Si waveguide), 60 µm (transition – from top to bottom taper section) and 180 µm (output - SiN waveguide) are shown as inset figures. c) The simulated coupling efficiency for the optimal designed taper dimensions and 200 nm oxide.

To demonstrate this fast adiabatic coupling, we fabricated a two-tier Si taper design with the thicknesses of 150nm for both the top and bottom sections. The lengths of the top and bottom taper are 60 µm and 120 µm respectively and the tip-width of both the taper sections is 120 nm. This two-tier Si taper is separated by a 200nm oxide layer from the SiN waveguide of 1 µm width and 600 nm thickness. These geometric parameters were chosen by optimising the coupling effeciency of the fundamental TE mode between the Si taper and SiN waveguide using finite-difference eigenmode (FDE) simulations in FIMMWAVE by Photon Design.

In Fig 1 (b), we show the simulated coupling efficiency (red colour) and the corresponding effective refractive index (blue colour) of the fundamental TE mode plotted against the length of the above described two-tier Si taper. During the simulation, the input is launched in the Si waveguide and the output is collected from the SiN waveguide. It can be noticed that the effective refractive index of the mode descreases as the width of the Si taper decreases in the propagation direction (*Z*-axis). At 60 µm, where the top section of the taper ends, the effective refractive index of the mode decreases dramatically as indicated by the green circle in Fig. 1 (b). This sharp transition allows efficient coupling for taper lengths as small as 180 µm. To show this effiecient coupling mechanism, the optical mode profile at *Z*=0 µm (input - Si waveguide), *Z*=60 µm (transition – from top to bottom taper section) and *Z*=180 µm (output - SiN waveguide) lengths are shown as inset figures in Fig 1 (b).

The proposed vertical coupler design, based on a spot size-converter (SSC), is highly tolerant to the fabrication imperfections such as SiN waveguide misalignment. In Fig 1 (c), we show the coupling efficiency versus the length of bottom section of the coupler for two different coupler systems. The blue line in Fig 1(c) indicates the coupling efficiency of a coupler design that has perfect alignment between the Si-taper and SiN waveguide along the lateral direction. On the other hand, the green line indicates the coupling efficiency of a coupler design where SiN waveguide is shifted 200nm away from the Si taper along the lateral direction. It is clear from Fig 1. (c) that in these vertical couplers, such horizontal misalignments has a negligble effect on the coupling efficency, while such large misalignment might pose a significant problem for in-plane couplers. For these practial reasons, the two-tier vertical coupling structures can be much more effiective than in-plane (horizontal) coupling structures.

2. Fabrication

The SSCs are fabricated on a SOI wafer (300 nm thick Si on top of a 2 µm buried oxide as shown in Fig. 2 (a)) in a two-step lithography. In the first step, the top taper structure is defined, followed by a 300nm Si etching as shown in Fig. 2 (b). In the second step, the bottom taper is defined, followed by 150nm Si etch as shown in the Fig. 2 (c). All lithography steps are performed using deep ultraviolet (DUV) 193 nm lithography [16]. The taper tip width is about 120 nm in both cases and it is limited by the DUV lithography resolution.

The SiN and Si layers are separated vertically by a SiO_2 intermediate layer as shown in Fig. 2 (d). As this spacing layer forms part of the coupling structure, a high optical quality layer is necessary. This silicon dioxide layer is deposited by high-density plasma deposition (HDP). Furthermore, Chemical mechanical polishing (CMP), is used to planarize the oxide surface and thin down the film to the targeted thicknesses.

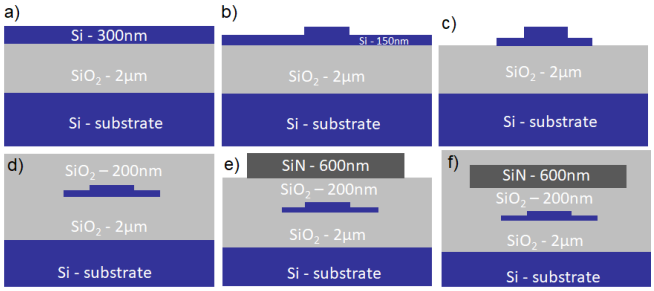
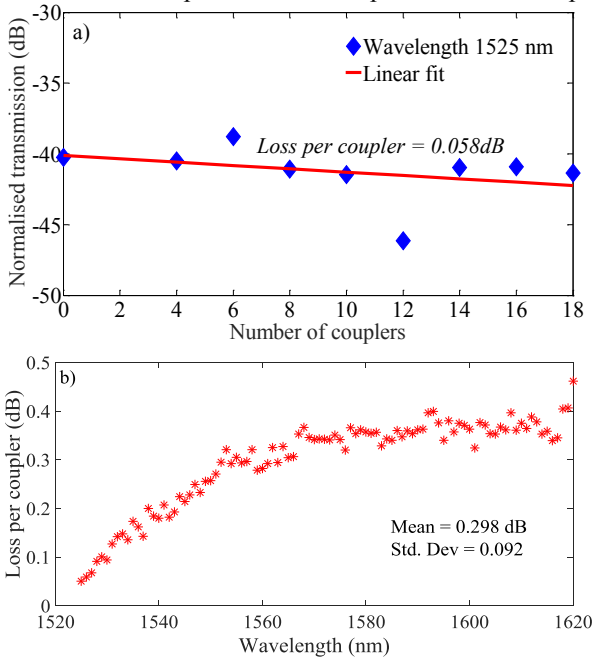


Figure 2: A cross-sectional view of the vertical integrated SSC with SiN waveguide. a) A standard 200 mm SOI wafer. b) First step Si patterened to define the top taper (after 150 nm Si etch). c) Second step Si patterened and etched to define the bottom taper. d) After 200 nm thick oxide deposition on top of the SSC. e) 600 nm PECVD SiN is deposited and the waveguide is patterned and etched. f) After 2 µm of SiO_2 encapsulation.

On top of this polished oxide surface, a low-stress, non-stoichiometric, SiN is deposited at 300°C, using plasma enhanced chemical vapour deposition (PECVD). The thickness of the deposited SiN is 600 nm. The SiN waveguide of 1µm width is then defined using 248nm DUV lithography and etched by RIE using a CF_4-CH_2F_2-O_2 mixture. The SiN waveguide is used as both input and ouput waveguide, to couple the optical mode back and forth into the Si layer through the SSCs. The waveguides dimension of both SiN and Si are optimised for TE single mode operation at 1550 nm, to avoid the power coupling into the higher order modes. Finally, the entire wafer is covered by SiO_2 to serve as a top cladding layer.

3 Results and Discussions

The SSCs are characterised using an 'end-fire' experimental setup. This set-up consists of a amplified spontaneous emission (ASE) broadband source (Amonics, ALS-CL-15-B-FA), a polarization beam splitter to select the TE polarization, collimation optics and an optical spectrum analyser (Yenista, OSA20). Our devices are fabricated during the same fabrication run as [16],where the measured propagation loss for the Si rib waveguide (slab 150nm thick) is 1.9 dB/cm and for the strip SiN waveguide it is 0.8 dB/cm at 1310 nm. The measured facet coupling loss is 7 dB/facet. We used the blank SiN waveguide to extract the coupling loss from the total experimental insertion loss. To evalaute the loss per coupler, we fabricated nine devices, with an increasing number of SSC pairs (from 1 to 9). In Fig. 3 (a), we plot the transmission versus the number of SSCs at a wavelength of 1525nm for a 180nm thick intermediate layer. We note that while this differs slightly from the afformentioned design value (200 nm) our simulations show that there is no performance difference between these two spacing layer thicknesses, see Fig. 3(c) It is evident from Fig 3(a), that the loss per SSC is as low as 0.058 dB, which is remarakable. Fig. 3 (b) shows the spectral response of the loss per coupler. It can be noticed that in the entire 100nm bandwidth, covering both the C and L-bands, the average loss per coupler is only 0.298 dB. Fig. 3(b) also shows that the loss increases with increasing wavelength, simulations predict a flat wavelength response and we therefore attribute this increase in loss to scattering caused by the Si tip roughness. The wavelength-dependency of the coupling loss can be further reduced by using a nonlinear tapering profile such as an exponential taper, which reduces the structured dispersion loss compared to a linear taper.



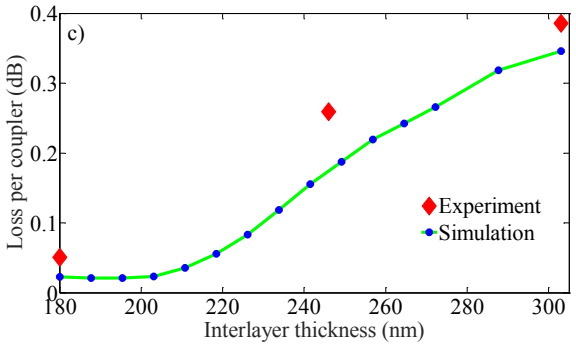


Figure 3: a) Normalised transmission values (at 1525nm operating wavelength) for different number of SSCs from 0 to 18 (experimental measurements, blue diamonds, and linear fit, red line). The coupling loss is 0.058dB/SSC. b) Loss per SSC for different wavelengths. The mean loss over the 100 nm bandwidth in the C and L-bands is 0.298dB/SSC. c) Measured (red diamonds) and simulated (blue dots) coupling loss per SSC for varying oxide thickness.

Furthermore, to study the effect of intermediate layer thickness, devices with three different oxide thickness i.e 180 nm, 246 nm and 303 nm were fabricated. These oxide thickness values were determined by ellipsometry. For the designed taper dimensions, a higher coupling loss is expected for thicker oxide layers. As the oxide thickness increases, the overlap between the evanescent tails of the optical mode is reduced and coupling becomes less efficient. The measured coupling loss for all three thicknesses agrees well with the simulated value, as shown in Fig. 3 (c).

The coupling efficiency of the spot size converter also depends on the taper dimensions, e.g. the taper length and tip width. Therefore, we experimentally studied the effect of different taper lengths (tl) for a constant tip width (tw, 120 nm) and different tip widths for a constant taper length of 180 µm (i.e. a 60 µm top taper plus a 120 µm bottom taper). In Fig. 4 (a) and (b) the increasing trend in transmission of the devices is due to the absorption of N-H bond centered at C-band, also observed in [18], [19], [21]. From Fig. 4 (a), it is evident that the coupling efficiency increases with an increase in the taper length, from 30 µm up to 120 µm. For any further increase in taper length beyond 120 µm, there is no change in the coupling efficiency. From Fig. 4 (b), it can be seen that for a constant taper length of 180 µm, different tip widths do not influence the coupling efficiency of the optical mode significantly. However, at wider tip width of 300 nm, they can cause a Fabry-Perot oscillations due to light being reflected at the bottom taper interfaces.

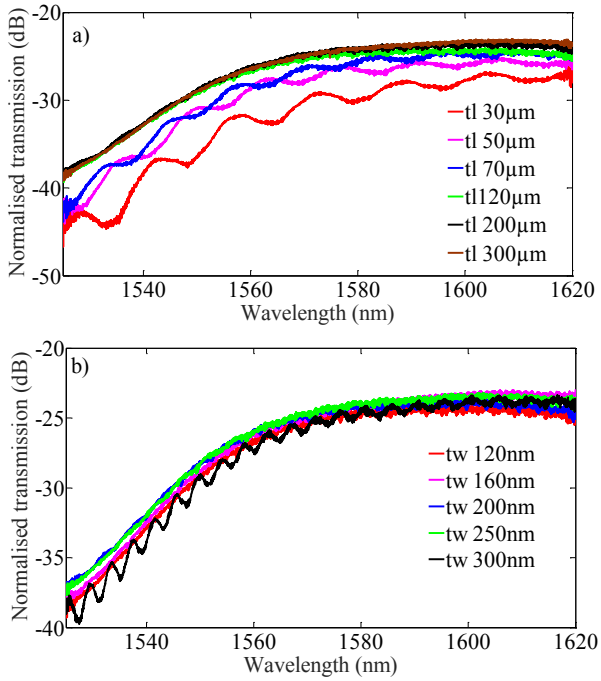


Figure 4: a) Experimentally measured transmission spectrum of the SSCs for different bottom taper lengths (tl), from 30 µm to 300 µm (the top taper length kept constant at 60 µm), with a constant tip width of 120 nm. b) Transmission spectrum of the SSCs for different taper tip widths from 120 nm to 300 nm at constant taper length of 180 µm.

Table 1 summarises the layer-to-layer coupling loss of monolithic integrated SiN platform in various configurations and our results are benchmarked with the start-of-the-art.

4. Conclusion

We have designed and demonstrated a compact two-tier taper for efficient coupling of light between the Si and SiN layers. We achieved coupling loss as low as 0.058 dB ± 0.01 dB per transition at 1525 nm and an average coupling loss of 0.298 dB/SSC over 100 nm bandwidth in the C and L- bands. Furthermore, the dimensions of the two-tier Si tapers and the intermediate layer thickness are studied to optimise the coupling efficiency. The two-tier taper coupler will allow the vertical integration of silicon and silicon nitride, key for future integrated photonics circuits.

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[1] Cisco 2017 The Zettabyte Era: Trends and Analysis White Papers [online] 1465272001812119 available: https://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/vni-hyperconnectivity-wp.html

[2] Atabaki A H, Moazeni S, Pavanello F, Gevorgyan H, Notaros J, Alloatti L, Wade M T, Sun C, Kruger S A and Meng H 2018 Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip Nature 556 349

[3] Reed G T, Mashanovich G Z, Gardes F Y, Nedeljkovic M, Hu Y, Thomson D J, Li K, Wilson P R, Chen S W and Hsu S S 2014 Recent breakthroughs in carrier depletion based silicon optical modulators Nanophotonics 3 229–45

[4] Debnath K, Gardes F Y, Knights A P, Reed G T, Krauss T F and L. O'Faolain 2013 Dielectric waveguide vertically coupled to all-silicon photodiodes operating at telecommunication wavelengths Appl. Phys. Lett. 102 171106

[5] Ma Y, Zhang Y, Yang S, Novack A, Ding R, Lim A E-J, Lo G-Q, Baehr-Jones T and Hochberg M 2013 Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect Opt. Express 21 29374

[6] Kiyat I and Aydinli A 2005 High-Q silicon-on-insulator optical rib waveguide racetrack resonators Opt. Express 13 1900–5

[7] Kiyat I and Aydinli A 2005 High-Q silicon-on-insulator optical rib waveguide racetrack resonators Opt. Express 13 1900–5

[8] Maegami Y, Takei R, Omoda E, Amano T, Okano M, Mori M, Kamei T and Sakakibara Y 2015 Spot-size converter with a SiO2 spacer layer between tapered Si and SiON waveguides for fiber-to-chip coupling Opt. Express 23 21287

[9] Kim G-D, Lee H-S, Park C-H, Lee S-S, Lim B T, Bae H K and Lee W-G 2010 Silicon photonic temperature sensor employing a ring resonator manufactured using a standard CMOS process Opt. Express 18 22215

[10] Shang K, Pathak S, Qin C and Yoo S J B 2017 Low-Loss Compact Silicon Nitride Arrayed Waveguide Gratings for Photonic Integrated Circuits IEEE Photonics, vol. 9, 1943-0655

[11] S. Iadanza, A. P. Bakoz, P. K. J. Singaravelu, D. Panettieri, S. A. Schulz, G. C. R. Devarapu, S. Guerber, C. Baudot, F. Boeuf, S. Hegarty and L. O'Faolain 2018 Thermally stable hybrid cavity laser based on silicon nitride gratings Appl. Opt. 57(22), E218-E223

[12] L. Stefan, M. Bernard, R. Guider, G. Pucker, L. Pavesi, and M. Ghulinyan 2015 Ultra-high-Q thin-silicon nitride strip-loaded ring resonators Opt. Lett. 40, 3316-3319

[13] Kapil Debnath, Thalia Dominguez Bucio, Abdelrahman Al-Attili, Ali Z. Khokhar, Shinichi Saito and Freceric Y. Gardes

2017 Photonic crystal waveguides on silicon rich nitride platform Opt. Express 25, 3214-3221
[14] Sun R, Beals M, Pomerene A, Cheng J, Hong C-Y, Kimerling L and Michel J 2008 Impedance matching vertical optical waveguide couplers for dense high index contrast circuits. Opt. Express 16 11682–90
[15] Hatori N, Shimizu T, Okano M, Ishizaka M, Yamamoto T, Urino Y, Mori M, Nakamura T and Arakawa Y 2014 A Hybrid Integrated Light Source on a Silicon Platform Using a Trident Spot-Size Converter J. Light. Technol. 32 1329–36
[16] Wilmart, Q., D. Fowler, C. Sciancalepore, K. Hassan, S. Plantier, L. Adelmini, S. Garcia, D. Robin-Brosse, S. Malhouitre, and S. Olivier 2018 A hybrid SOI/SiN photonic platform for high-speed and temperature-insensitive CWDM optical transceivers. International Society for Optics and Photonics, In Silicon Photonics XIII, vol. 10537, p. 1053709
[17] Strain, M.J.< & Sorel, M. 2007 Compact Semiconductor Tapers for Deep to shallow Etch Transitions. IEEE Photonics Technology Letters, 19(19), 1544-1546
[18] Sherwood-Droz, N., & Lipson, M. 2011 Scalable 3D dense integration of photonics on bulk silicon. Optics Express, 19(18), 17758
[19] Huang, Y., Song, J., Luo, X., Liow, T.-Y., & Lo, G.-Q. 2014 CMOS compatible monolithic multi-layer Si_3N_4-on-SOI platform for low-loss high performance silicon photonics dense integration. Optics Express, 22(18), 21859
[20] SMaegami, Y., Takei, R., Omoda, E., Amano, T., Okano, M., Mori, M., … Sakakibara, Y. 2015 Spot-size converter with a SiO_2 spacer layer between tapered Si and SiON waveguides for fiber-to-chip coupling. Optics Express, 23(16), 21287
[21] Poon, J. K. S., & Sacher, W. D. 2017 Multilayer silicon nitride-on-silicon photonic platforms for three-dimensional integrated photonic devices and circuits. Device Research Conference - Conference Digest, DRC, 33(4), 901–910