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Design and Implementation of a Micro-Inverter for Photovoltaic Applications

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DESIGN AND IMPLEMENTATION OF A MICRO-INVERTER FOR PHOTOVOLTAIC APPLICATIONS

CHI-THANG PHAN-TAN

DESIGN AND IMPLEMENTATION OF A MICRO-INVERTER FOR PHOTOVOLTAIC APPLICATIONS

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Submitted in fulfillment of the degree of
Master of Engineering by Research in Electrical Engineering

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Cork Institute of Technology, November, 2017

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DECLARATION

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person nor material to a substantial extent has been accepted for the award of any other degree or diploma by a university of higher learning, except where due acknowledge has been made in the text.

Signature of author: ……..

Certified by: ……..

Date: ……..

ABSTRACT

The objective of this work is to design and build a novel topology of a micro-inverter to directly convert DC power from a photovoltaic module to AC power. In the proposed micro-inverter, a structure with two power stages, which are DC/DC and then DC/AC converters, is used. The inverter is designed capable for future integration of battery as a buffer in between the DC/DC and DC/AC converters.

A novel MPPT algorithm is implemented and evaluated in the DC/DC converter to optimize the solar panel energy production. The new method operates with an efficiency of 99.23%, which is a 2.5% improvement on the standard method, and a response time of less than 0.2s.

A modification of designing the inductor and transformer using Litz wires is also mentioned. The core using Litz wires may reduce the Eddy current effect and is 15% smaller than the coil using a single conductor.

In this research, the following approach is taken. A literature review was conducted, to identify potential converter topologies. A topology for both converters was selected by comparison of performance through simulations. Maximum Power Point Tracking algorithms were also investigated, to select an appropriate control scheme. A design for two converters was then performed, leading to a prototype for experimental verification.

TABLE OF CONTENT

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

AC	Alternative Current
ADC	Analog to Digital Converter
BS-P&O	Binary-Search-Based Perturb and Observe method
BST	Bisection search theorem
CCC	Charge Control Circuit
CCS	Code Composer Studio (integrated development environment)
CIDBI	Couple-inductor double-boost inverter
DC	Direct Current
FFT	Fast Fourier Transform
HCMC	Hysteretic Current Mode Control
HF	High-Frequency
HV	High Voltage
ICDI	In-circuit Debug Interface
INC	Incremental Conduction method
LC filter	Filter which has an inductor (L) and a capacitor (C) connected to each other
LPF	Low-pass filter
LV	Low Voltage
MEB	Multilevel Energy Buffer
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MLT	Mean Length of a Turn of winding wires
Op-amp	Operational Amplifier
P&O	Perturb and Observe method
PCB	Printed Circuit Board
PV	Photovoltaic
PWM	Pule-Width-Modulation
RMS	Root-Mean-Square value
SCEB	Switched-Capacitor Energy Buffer
SEPIC	Single-Ended Primary-Inductor Converter
SPWM	Sinusoidal Pule-Width-Modulation
STC	Standard Test Condition
THD	Total Harmonic Distortion
ZCD	Zero-crossing Detector

NOMENCLATURE

INDUCTOR and TRANSFORMER DESIGNING SECTION

Label	Description	Unit
A_c	cross-sectional area of the core	m^2
A_L	induction factor	H
A_{Litz}	overall cross-sectional area of a Litz wire	m^2
A_p	product of A_c and A_{wd}	m^4
A_{stand}	strand wire area	m^2
A_{stand_p}	strand wire area of primary side of transformer	m^2
A_{stand_s}	strand wire area of secondary side of transformer	m^2
A_t	surface area of core	m^2
A_w	overall cross-sectional area of the winding	m^2
A_{wd}	window area of core for winding	m^2
B_{max}	maximum flux density (typical $B_{max} \approx (0.6 - 0.7)B_{sat}$)	T
B_o	optimum flux density of transformer	T
B_{sat}	saturation flux density	T
ΔB	flux density ripple	T
d_{stand}	strand wire diameter	m
f	frequency of current	Hz
N	number of turns of inductor	1
N_p	number of primary turns of transformer	1
N_s	number of secondary turns of transformer	1
n_{Litz}	number of Litz wires of inductor	1
n_{Litz_p}	number of Litz wires of primary side of transformer	1
n_{Litz_s}	number of Litz wires of secondary side of transformer	1
h_c	heat transfer coefficient (typical $h_c = 10$)	W/m^2 °C
I_{L_max}	maximum current of inductor	A
I_{L_rms}	RMS of inductor current	A
I_{rms_p}	RMS current of primary side of transformer	A
I_{rms_s}	RMS current of secondary side of transformer	A
J_0	current density	A/m^2
k_a	coefficient; $k_a = A_t/A_p^{1/2}$ (typical $k_a = 40$)	1
k_c	coefficient; $k_c = V_c/A_p^{3/4}$ (typical $k_c = 5.6$)	1
k_{core}	material parameter (N87 material $k_c = 16.9$)	1
k_i	current coefficient; $k_i = I_{L\_rms}/I_{L\_max}$	1
k_g	air gap correction coefficient	1
k_t	coefficient (typical $k_t = 48.2 \times 10^3$)	$(A^2/m^3$ °C$)^{1/2}$
k_u	window utilization factor; $k_u = A_w/A_{wd}$	1

k_v	waveform factor	1
k_w	coefficient; $k_w = V_w/A_p^{3/4}$ (typical $k_w = 10$)	1
L	needed inductance	H
l_c	effective magnetic path length	M
l_g	length of the air gap	M
l_{turn}	mean length of a turn (MLT) of winding wires	M
P_{core}	power loss of the core	W
P_D	maximum dissipation power of the core	W
P_{in}	input power of transformer	W
P_{loss}	total power loss of the inductor; $P_{loss} = P_{core} + P_{wire}$	W
P_{wire}	power loss of the winding wire	W
R_{wire}	resistance of the copper winding wire	Ω
R_{wire_p}	resistance of the copper winding wire in primary side	Ω
R_{wire_s}	resistance of the copper winding wire in secondary side	Ω
R_θ	thermal resistance of the core	°C/W
$\mathcal{R}_{eq}$	equivalent magnetic reluctance	1/H
$\mathcal{R}_c$	magnetic reluctance of the core	1/H
$\mathcal{R}_g$	magnetic reluctance of the air gap	1/H
T	Temperature	°C
T_{max}	maximum temperature; $T_{max} = T + \Delta T$	°C
ΔT	temperature rise	°C
V_c	volume of the core	m^3
V_{rms_p}	RMS voltage of primary side of transformer	V
V_w	volume of the winding	m^3
α	material parameter (N87 material $\alpha = 1.25$)	1
α_0	temperature coeff. of resistivity at 20°C ($\alpha_{0\_cu} = 0.004$)	1/°C
β	material parameter (N87 material $\beta = 2.35$)	1
γ	coefficient; $\gamma = P_{core}/P_{wire}$	1
δ	skin depth	M
μ_0	magnetic permeability of free space; $\mu_0 = 4\pi \times 10^{-7}$	H/m
μ_r	relative permeability	1
μ_e	effective relative permeability	1
μ_{e_opt}	optimum effective relative permeability	1
ρ	resistivity of conductor	Ωm
ρ_0	resistivity of conductor at 20°C ($\rho_{0\_cu} = 1.72 \times 10^{-8}$)	Ωm

CHAPTER 1. INTRODUCTION

In this section, the motivation to select the research topic is presented. The potential contributions of this research are outlined and the method of conducting the research is also shown.

1.1. Micro-inverter

1.1.1. Introduction

Energy sources are amongst the most important challenges facing both the world's industrialized and developing countries. The amount of fossil fuel is now decreasing and this kind of energy causes a lot of environmental problems. Renewable or green energy is therefore being developed at high speed recently, especially solar energy. One of methods to harvest the solar energy is using the photovoltaic (PV) modules, which absorb the sun's photonic energy and transfer it to electricity with a p-n junction. In comparison to other kinds of renewable energy systems, there is no moving part in a solar system, which means that the solar systems may last for a long time with minimum maintenance [1].

In PV systems, inverters are used for converting DC from a solar panel to AC to connect directly to the utility grid. Inverters used in PV applications in the market are mainly configured in central and string formats with the power ratings above 5kW. Residential PV projects are increasing because of the steadily decreasing prices of solar installations and devices [2]. This requires other kinds of inverter with low power rating. Micro-inverters are designed for use of low power input. The micro-inverter converts DC to AC and connects to the grid from a solar module whose maximum power rating is about 350W.

Micro-inverters have many advantages in comparison with string-inverters [3]. As reported in [4], micro-inverters supply 11.36% higher energy output than string-inverters in the case of partial shading. In clear sky condition, micro-inverters produce 20% more power than string inverters [5]. Inverters are the most unreliable components in solar systems [6], and the micro-inverters should be more desirable than string-inverters with failure rates are lower than that of string-inverters [1]. Moreover, according to [1] the cost of installing a system, including equipment, maintenance and labor, using string-inverters is higher than that of a system with micro-inverters. Another aspect to be considered is safety, where high DC voltage is the likely cause of arc faults and can also sustain arcs better than AC

voltage [7][8]. Since the operating DC voltage of micro-inverters is much lower than string-inverters, the micro-inverter should lower the risk of arc faults or system fires [1][9]. In comparison to string-inverters, micro-inverters are simpler, as they deal with a lower power range [10]. In addition, the flexibility of PV systems could be increased by avoiding connecting several solar modules into strings.

1.1.2. Topology

The purpose of this research is to design a micro-inverter which can integrate a small battery. The reasons for designing a topology which is capable for a battery to be a buffer are introduced as the following. First, in comparison to capacitors, the capacity of a battery is higher. As seen in Figure 1.1, the batteries have larger energy density than capacitors, this means in the same size and weight, the batteries can store larger amount of energy than the capacitors. Second, the batteries can also be used as a power supply for the control circuit at night while there is no power from the sun. Third, the batteries can balance the input and output of the inverter by storing or supplying energy. These features of batteries can be used for smart inverters in micro-grid and smart-grid applications [11][12][13].

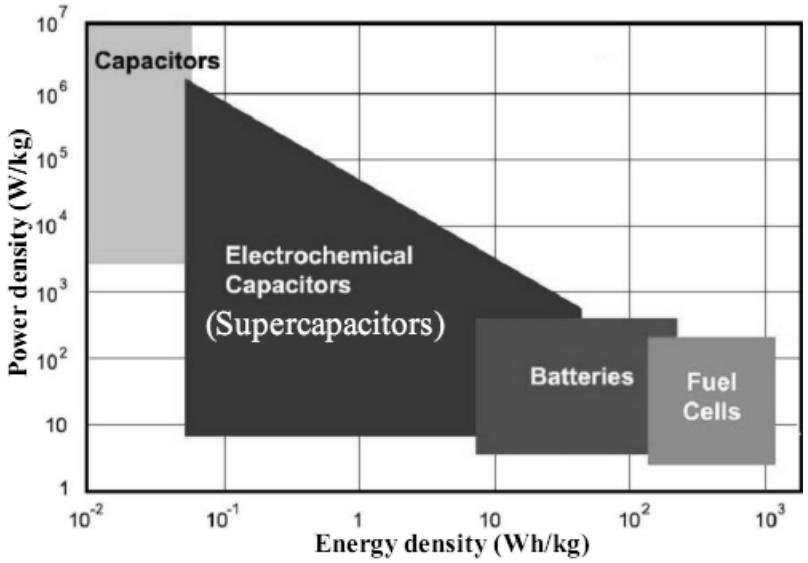

Figure 1.1: Power density vs. energy density of various energy storage systems [14]

The design difference between the string inverter and micro-inverter is the DC input voltage. As seen in Figure 1.2(a), the input of string inverter is an array of PV panels. The input of the inverter is usually up to 600V, the inverter does not need to increase the voltage to grid level, therefore the DC/DC and DC/AC topologies are simple. For instance, the DC/AC circuit is just a H-bridge of four switches.

The input of a micro-inverter is around 30V while its output is over 350V-peak. Therefore, a transformer is needed to boost low input voltage to grid level. The common topology of micro-inverter is shown in Figure 1.2(b). The low input voltage is boosted to high DC voltage by a DC/DC converter integrated with a high-frequency transformer (typical topologies of this DC/DC converter are presented in Figure 2.1). The DC buffer is usually made of capacitors of high-voltage rating.

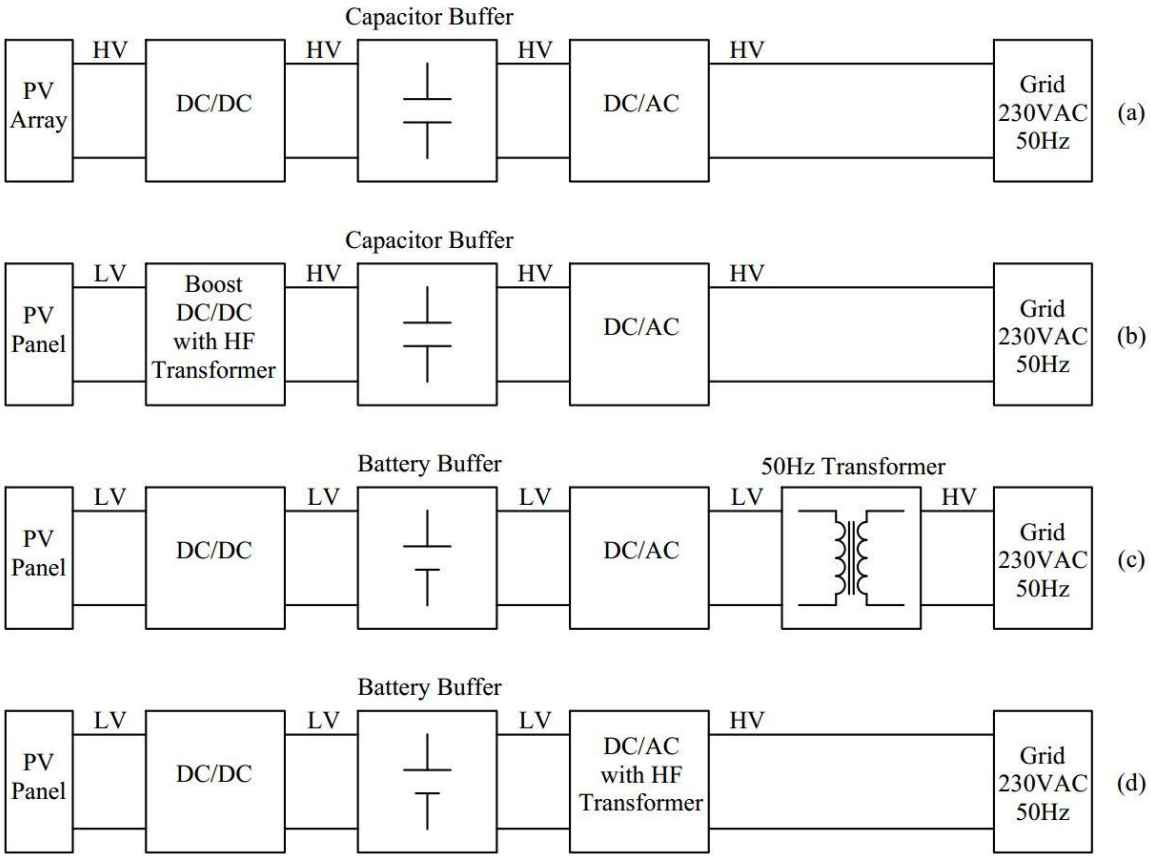

Figure 1.2: Two-stage PV inverter topologies

(a) String inverter (b) Micro-inverter with capacitor buffer
(c) Micro-inverter with battery buffer and low-frequency transformer
(d) Micro-inverter with battery buffer and high-frequency transformer

As mentioned, the goal of this research is to integrate a battery. However, the battery voltage is low, for example a Li-ion cell is 3.7V, so that to make higher voltage, several cells are connected in series. By putting the battery in the DC-link, the topology of micro-inverter is presented in Figure 1.2(c). The micro-inverter has similar topology to the two-stage string inverter. After the DC/AC converter, the 50Hz low voltage AC will pass through a transformer to boost the voltage to grid level. However, it is known that the

lower the frequency, the larger the transformer. Hence, the 50Hz transformer is large in comparison to the size of the inverter.

Another approach is shown in Figure 1.2(d). The power flow is similar to the topology in Figure 1.2(c), but in the DC/AC converter, a high-frequency transformer is integrated making the size of the transformer small enough for a micro-inverter. The power flow topology as shown in Figure 1.2(d) is adopted in this work.

1.2. Research Context and Contribution to the Research Field

The research is concerned about the design and construction of a micro-inverter, which takes maximum power from a solar module and produces AC power at the output. The research deals with the design of a power circuit and its control algorithms.

The power circuit composes of two parts, the DC/DC and the DC/AC converters. The DC/DC converter is responsible for obtaining the maximum power from the solar module. The DC/AC inverter produces AC power for the output load. The DC/DC converter should have a continuous input current for efficient power extraction. A high quality output will be needed for the inverter. For safety and compactness, a high frequency transformer is also used. The diagram of the micro-inverter structure is shown in Figure 1.3.

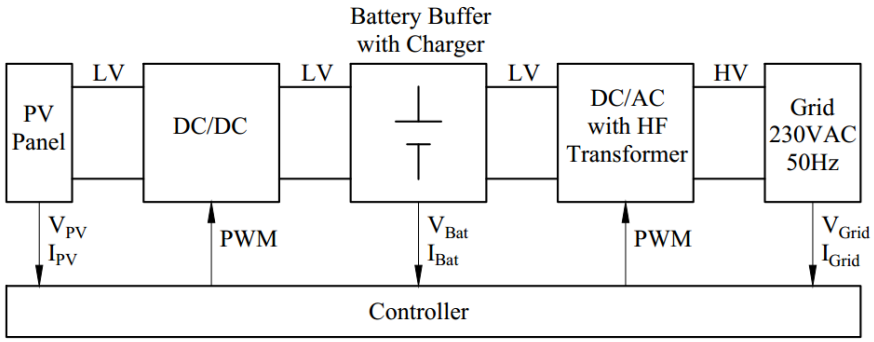

Figure 1.3: The block diagram of the micro-inverter

Contributions of the research to the general field research are:

- Selection of topologies for DC/DC and DC/AC converters.
- Design inverter topology which is able to integrate the battery as a buffer in between the DC/DC and DC/AC converter.
- A novel Maximum Power Point Tracking (MPPT) algorithm.
- Design inductors and transformer using Litz wires

The design of this inverter contributes a new control algorithm of MPPT for the PV applications. It also introduces a different type of DC/AC power circuit in which the high-

frequency transformer is applied with pule-width-modulation (PWM) waveform. In addition, it is the introduction for the inverter topology which is able to have a battery application in the future. Note that, the control of optimizing the use of the battery is beyond the scope of this thesis. The battery will be investigated later in other work. In this thesis, the topology of the DC/DC and DC/AC is the focus.

1.3. Research methodology

The methodology of this research is laboratory work consisting of experiment and simulation. The first task is literature review, which includes identifying suitable power topologies and control algorithms for the micro-inverter. It was made by reviewing papers from academic conferences and journals. After selecting the potential circuits and algorithms, simulations were conducted using MATLAB software. The final power and control schemes were chosen by comparing simulated performance and suitability. A hardware power circuit was built for experimental verification. Power components and measuring equipment were required for this task.

The micro-inverter is the combination of the DC/DC and the DC/AC converters. Therefore, this thesis is divided into two main parts which are DC/DC and DC/AC circuit designs. In Chapter 2, the review of topologies of the converters and the MPPT methods is introduced. The review is the basis for selecting the suitable converter topologies for the micro-inverter. Chapter 3 describes the design of the DC/DC converter from theory, simulation, implementation, programming to the experiment. One of the main parts of this chapter is the introduction of a novel MPPT algorithm which is based on the binary-searching method. This MPPT method is verified in the simulation and the experiment for a better performance in comparison to the conventional MPPT methods. The introduction of the inductor design using Litz wires is also described in detail. In Chapter 4, the DC/AC topology is presented. The DC/AC topology is analyzed and simulated for its operation. The sensor circuits for measuring the grid are also introduced in this chapter. The methodology in the programming and control of the microcontroller is described. Similar to the inductor design, the detailed development of a high frequency transformer design is presented in this chapter. The conclusion in Chapter 5 summarizes the achievements of the project and problems encountered in the design process. Also, the detailed code for the microcontroller is shown in the Appendix.

CHAPTER 2. STATE OF THE ART

In this section, the conventional topologies of DC/DC and DC/AC converters used for PV applications are presented. A review of algorithms for tracking the maximum power point (MPP) of a solar module is also presented. Finally, the state of the art for micro-inverter technology is reviewed and the main topologies and their characteristics are outlined.

2.1. DC/DC converter

There are many types of DC/DC converter, which are suitable for the PV applications. The main duty of the DC/DC converter is to track the MPP of PV panels. It does so by increasing or decreasing the duty cycle of one or several active switches.

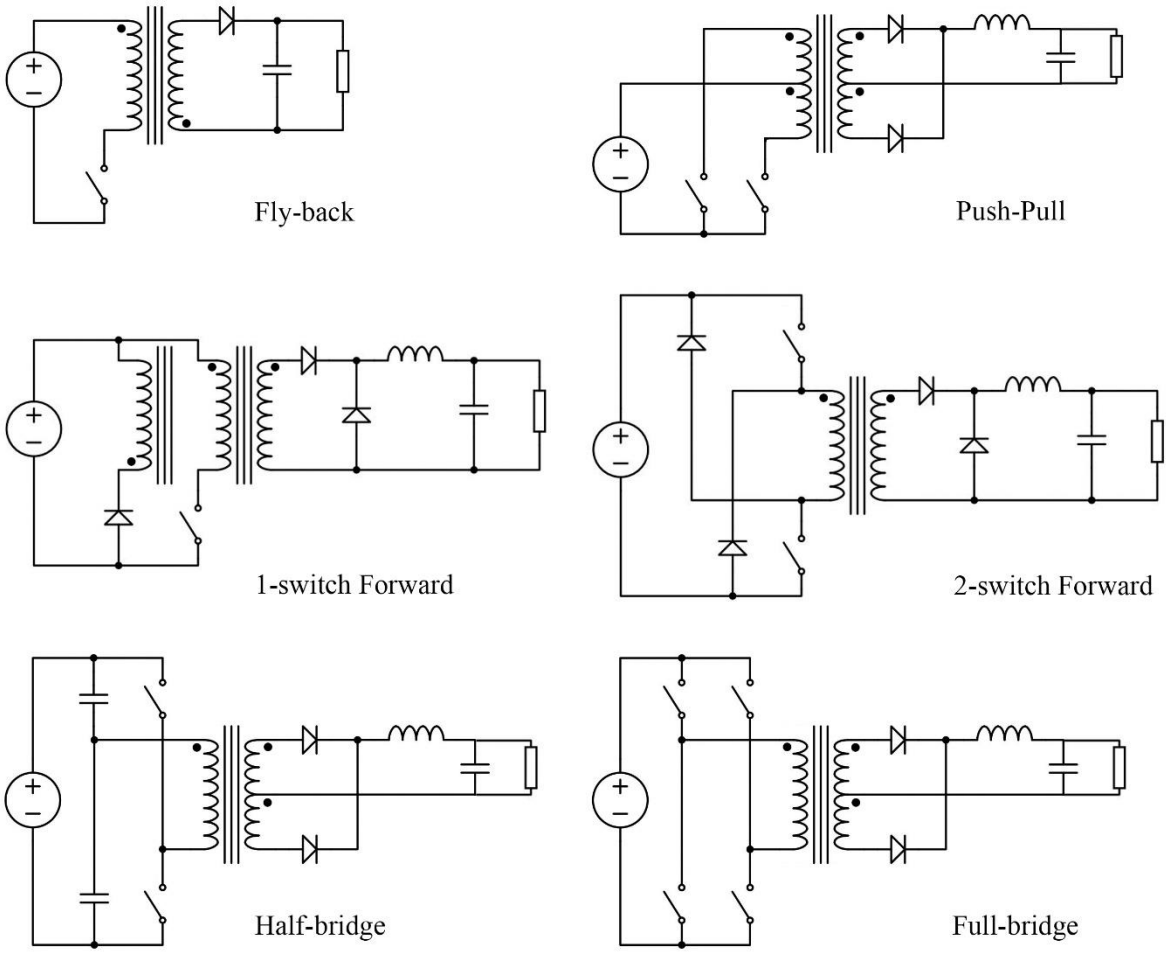

Figure 2.1: Isolating DC/DC converter topologies [15]

There are two main types of DC/DC converter. The first type is isolating converters with high-frequency transformers for isolation. The input and output of the converter are

electrically isolated by the transformer because the input and output are using separated ground connection. Moreover, the transformer has a function of boosting the low level input voltage to a higher level. There are many topologies for this kind of converter such as fly-back, push-pull, forward, half-bridge and full-bridge [15].

The isolating converter has the transformer which acts as an isolating component. In the isolating converter, the direct current is transformed to AC to pass through the transformer. After that, the power is rectified and a typical LC filter at the output takes the responsibility of filtering high frequency components. In addition, its output is at high voltage level, which helps the following DC/AC circuit to be designed smaller. However, the purpose of this project is to apply the battery buffer in between the DC/DC and DC/AC converters, so that the output of the converter should be low level and defined by the battery.

The second type of DC/DC converter is non-isolating converters. This type does not include a transformer so that it does not have magnetic and electrical isolation. Figure 2.2 shows the topologies of buck-boost DC/DC converters, which are able to make the output voltage lower or higher relative to the input voltage. Four typical topologies are buck-boost, Cuk, continuous input current buck-boost and SEPIC [15] [16].

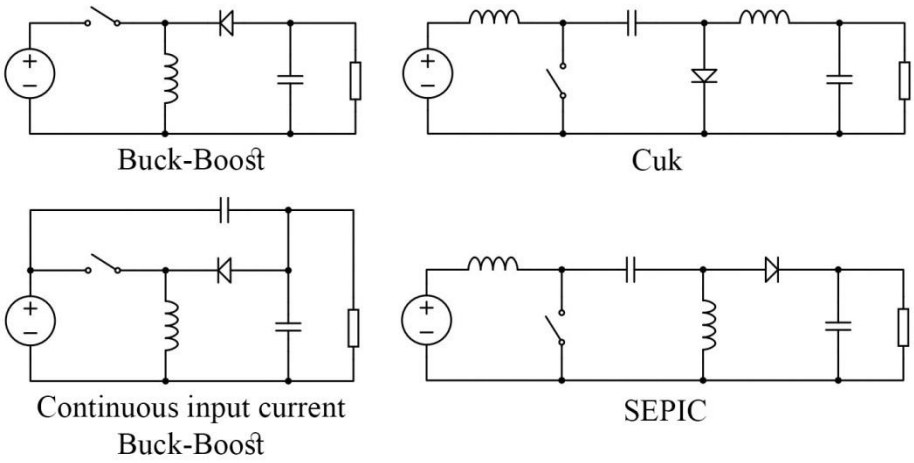

Figure 2.2: Non-isolating DC/DC converter topologies [15][16]

One compulsory requirement is that the output current of the PV, or the input current of the DC/DC converter, must be continuous. The continuous mode means that the input current of the converter will never go down to zero during the operation. In the case of discontinuous input current mode, the output current of PV panel is interrupted or goes down to zero which leads to the failure of getting maximum power. The buck-boost

converter has a switch in the input which means the input current would be interrupted or equal to zero when the switch is turned off. The buck-boost converter does not meet the continuous input current condition so that it is not chosen. The remaining three converters fulfill the requirement of continuous input current and they can buck or boost the input voltage as required by this project. However, output voltages of Cuk and continuous input current buck-boost converters are inversed with respect to the input voltages, leading to some difficulties in implementation. Therefore, we finally chose the SEPIC as the DC/DC converter for this application.

2.2. MPPT algorithms

In Figure 2.3, the typical characteristic I-V and P-V curves are shown at different irradiation values. It can be seen that with the higher irradiant, more power can be harvested from the solar panel. However, the operating power point may be anywhere in the P-V curve and it depends on the operating voltage of the panel. The energy of the solar panel should be converted as much as possible when it is available, and this can be done by applying MPPT algorithms. These methods are used to control the DC/DC converters to dynamically adapt its operating point to the MPP of the PV.

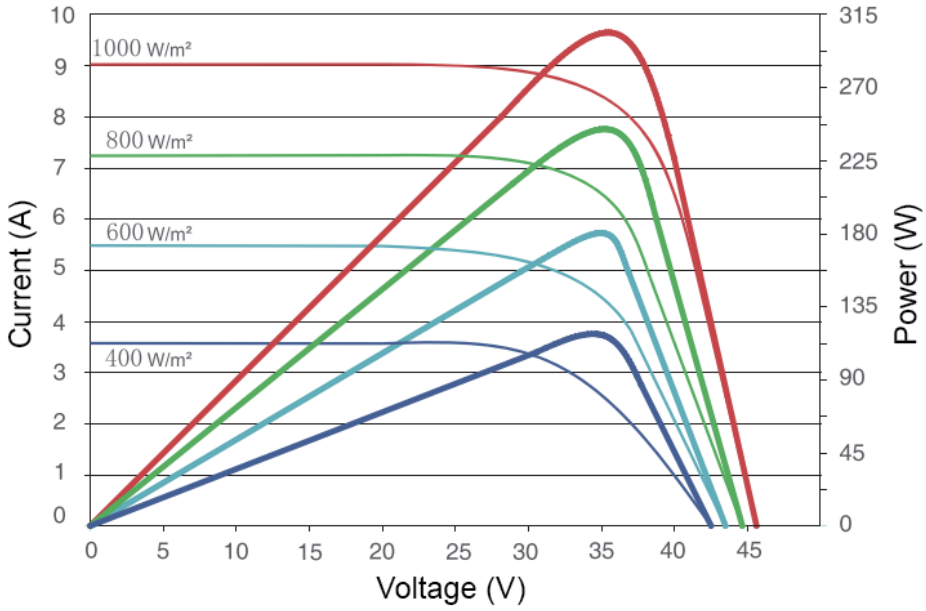

Figure 2.3: Typical PV Current-Voltage & Power-Voltage Curves [17]

There are many algorithms for finding the MPP of solar panels. Some methods are simple and easy to control such as: Fractional Open-Circuit Voltage V_{OC} [18], Fractional Short-Circuit Current I_{SC} [19], Perturb-and-Observe (P&O) [20][21][22] and the Incremental

Conductance (INC) [23][24][25]. However, there are complex methods for doing the task of tracking MPP [26][27] such as Current Sweep [28], Fuzzy Logic Control [29] and Artificial Neural Network [30]. These complex methods require a lot of calculations and memory, implying the need to use more powerful microcontrollers due to heavier computational load than that of simple methods. Hence, this project focuses on simple and effective MPPT method. The following is the detail explanation of two common MPPT algorithms P&O and INC, which will be mentioned on the later section.

2.2.1. Perturb and Observe method

One of the most popular ways of MPPT is the P&O method, with flowchart being shown in Figure 2.4.

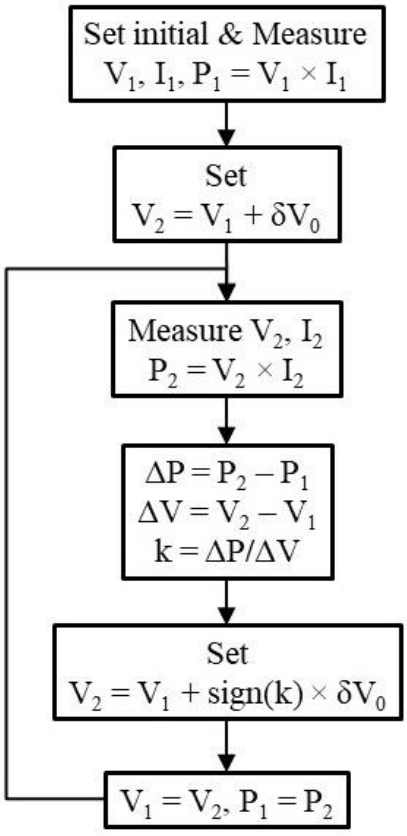

Figure 2.4: Flowchart of traditional Perturb & Observe method

The P&O is a straightforward, simple and fairly effective algorithm. In the initial state, the PV voltage V_1 and I_1 is measured. Then the voltage is changed by an amount of δV_0. The algorithm compares the previous power value to the current one. If there is difference, the controller will adjust the voltage by an amount of δV_0. The value of "k" is calculated to make the decision of increasing or decreasing the voltage. When the operation power point

is in the left of MPP, the value of "k" is positive and the voltage is increased to move closer to the MPP. And when the power point is in the right of MPP, the value of k is negative and the voltage is decreased. The efficiency of this algorithm depends on the perturbation size δV_0. The illustration is shown in Figure 2.5 and Figure 2.6 below.

Figure 2.5 shows the step δV_0 in small value. The operation point is started in the left of MPP and it takes many steps to reach the MPP.

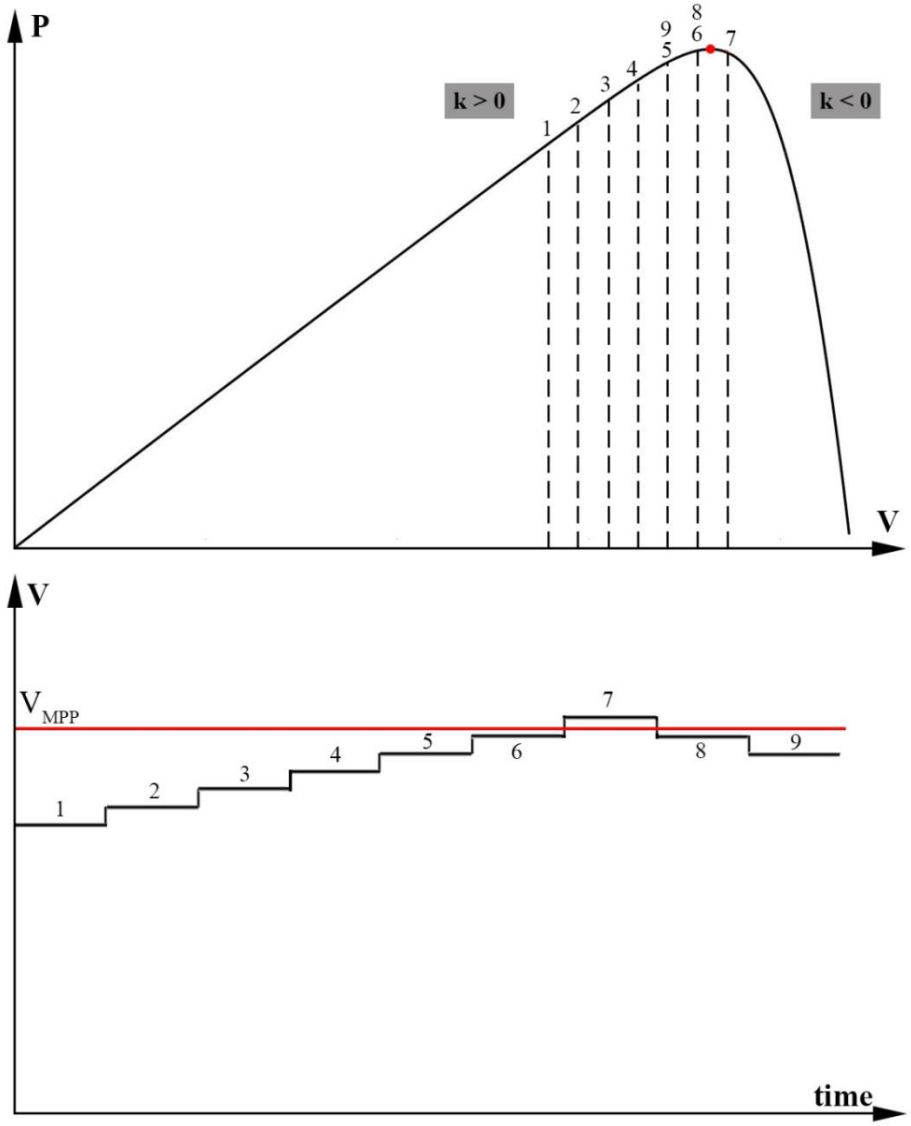

Figure 2.5: Illustration of P&O with small step

In Figure 2.6, when δV_0 is large, the algorithm can quickly move with large step but it cannot to find the exact MPP and the perturbation is higher with the larger δV_0.

In both cases of small and large δV_0 values, the power point cannot get to the MPP and just fluctuates around it. The second common MPPT algorithm is described in the next section.

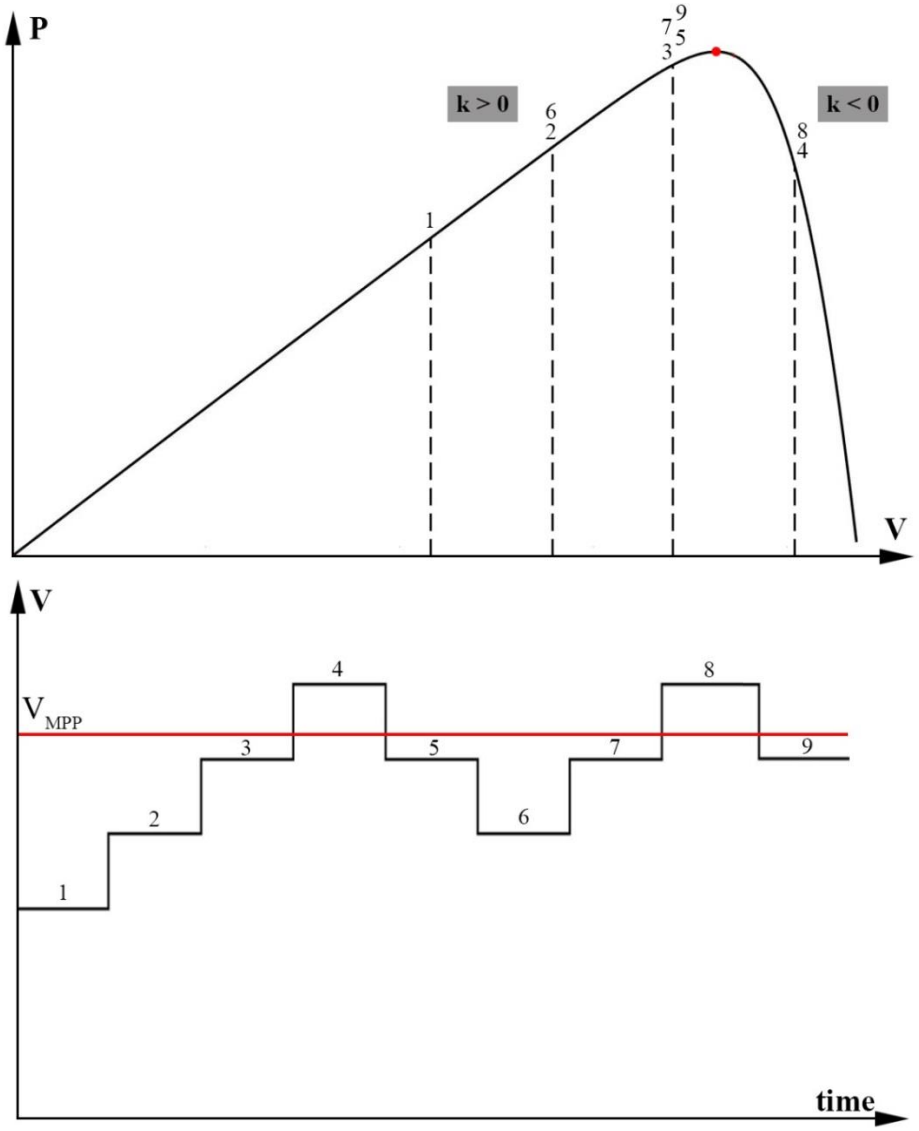

Figure 2.6: Illustration of P&O with large step

2.2.2. Incremental Conductance method

The second well-known algorithm of MPPT is the INC method. For this type of MPPT, the slope dP/dV of the P-V curve is used as the control variable. The slope is equal to zero at the MPP, positive on the left of MPP and negative on the right of MPP. The practical algorithm makes use of the approximation below, avoiding power calculations and derivations:

$$\frac{dP}{dV} = \frac{d(VI)}{dV} = I + V\frac{dI}{dV} \approx I + V\frac{\Delta I}{\Delta V} \tag{2.1}$$

Then it can be concluded that:

$$\begin{cases} dP/dV = 0 \\ dP/dV > 0 \\ dP/dV < 0 \end{cases} \rightarrow \begin{cases} \Delta I/\Delta V = -I/V & \text{at MPP} \\ \Delta I/\Delta V > -I/V & \text{left of MPP} \\ \Delta I/\Delta V < -I/V & \text{right of MPP} \end{cases} \quad (2.2)$$

This leads to the flowchart as shown in Figure 2.7.

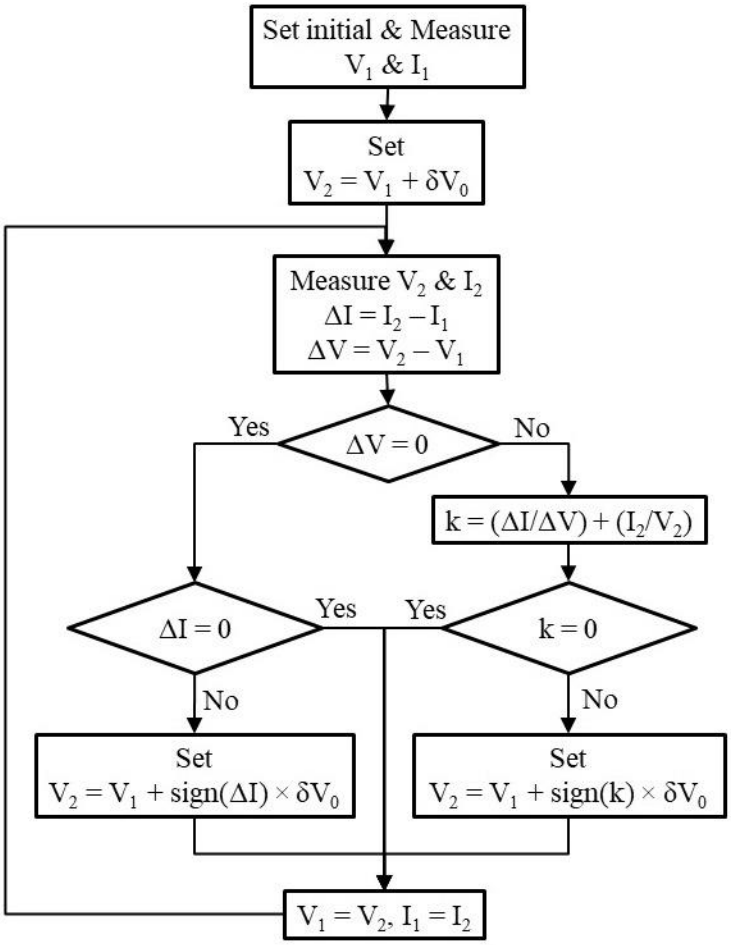

Figure 2.7: Flowchart of traditional Incremental Conductance method

This method has an advantage of keeping the voltage from constantly fluctuate and therefore can increase the overall efficiency. Similar to the P&O method, the INC method depends on the value of δV_0 or the perturbation of voltage is fixed to the values of δV_0.

2.3. Micro-inverter topology

Micro-inverters are just widely applied and commercially used from 2005. However, there are many topologies with advanced technologies and control, which are introduced in the following.

The common topology of a micro-inverter of solar companies is shown in Figure 2.8. It is a 2-stage system; the first stage is a DC/DC converter for getting the MPP. Then the output

voltage of DC/DC converter is boosted to a higher level by mean of a high frequency transformer. The second stage of the inverter is the DC/AC converter, which connects the output voltage to the utility grid. The isolation is achieved by a high-frequency transformer in DC/DC converter. A list of industrial micro-inverter manufacturers is shown in Table 2.1. In the table, the MPPT efficiency is the effectiveness of the MPPT algorithm. The overall efficiency of the inverter is the ratio between the PV input power and the grid output active power of the inverter. Also, the rating of those inverters is ranged from 200W to 380W.

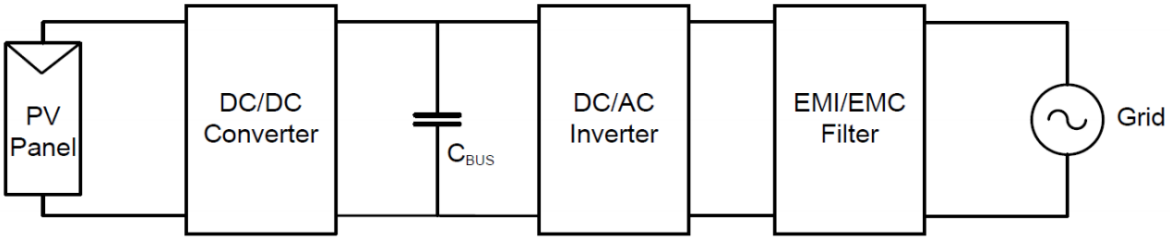

Figure 2.8: Block diagram of 2-stage micro-inverter [31]

Manufacturer	Efficiency		Maximum Power	
	MPPT	Overall	DC input	AC output
ABB [32]	-	96.5%	265W	250W
Darfon [33]	99.0%	94.1%	240W	220W
Enecsys [34]	-	95.4%	380W	340W
Enphase [35]	-	96.5%	350W	250W
Seimens [36]	99.4%	96.5%	270W	225W
Solarbridge [37]	-	95.5%	250W	225W
SMA [38]	-	95.9%	250W	240W
Freescale [31]	99.5%	93.0%	200W	200W

Table 2.1: Conventional commercial micro-inverter

In Figure 2.9, there is a single-stage inverter, which does both the MPPT and grid-connecting tasks through only one stage [39]. Hysteretic Current Mode Control (HCMC) technique is applied for modulating the L_1 current. This micro-inverter can both do MPPT from the solar panel and connect to the grid. The efficiency of this inverter is 93% with the sine wave output of 4.7% THD and the power factor of 0.98. Similar topologies for single-stage micro-inverter are also introduced in [40][41].

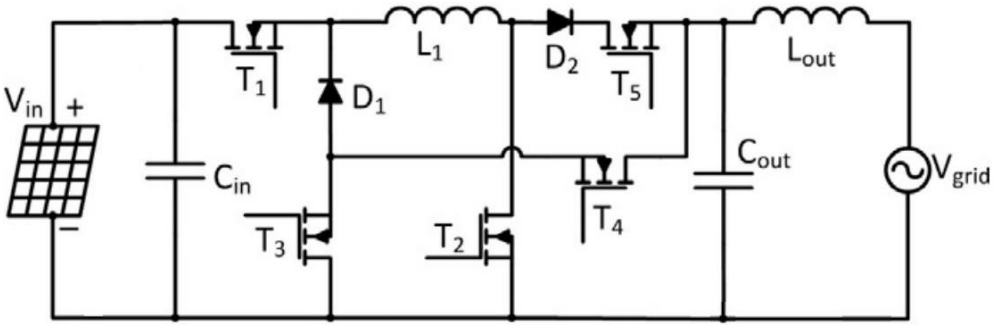

Figure 2.9: Single-stage micro-inverter [39]

The 2-stage inverter is represented in Figure 2.10. In the first stage-DC/DC-a haft-bridge of two switches is used for tracking the MPP. The efficiency of this topology is 98.2% at the power input of 210W [42][43].

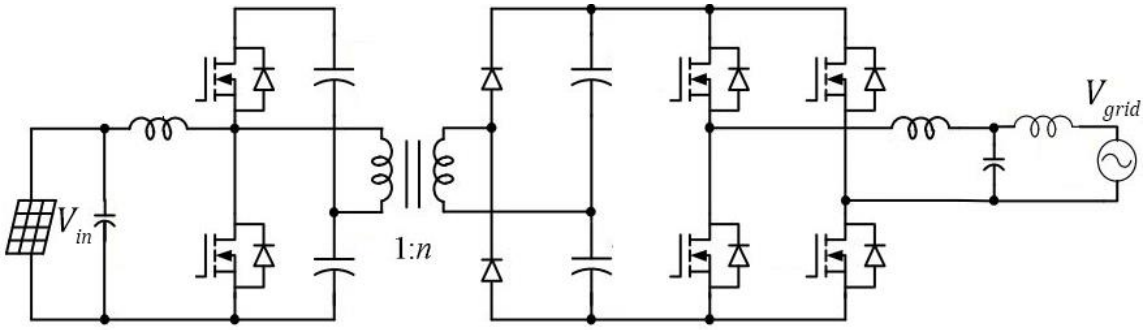

Figure 2.10: Boost half-bridge micro-inverter [42]

In Figure 2.11, the topology is the Couple-inductor double-boost inverter (CIDBI) [44]. It uses four switches for generating a sine wave and connecting to the grid. A DC source B_1 helps to increase the stability of the inverter. The experimental results for the power of 217.8W show the inverter's efficiency of 97.5% and total harmonic content of less than 3%. However, there is no isolation between the inverter and the utility grid.

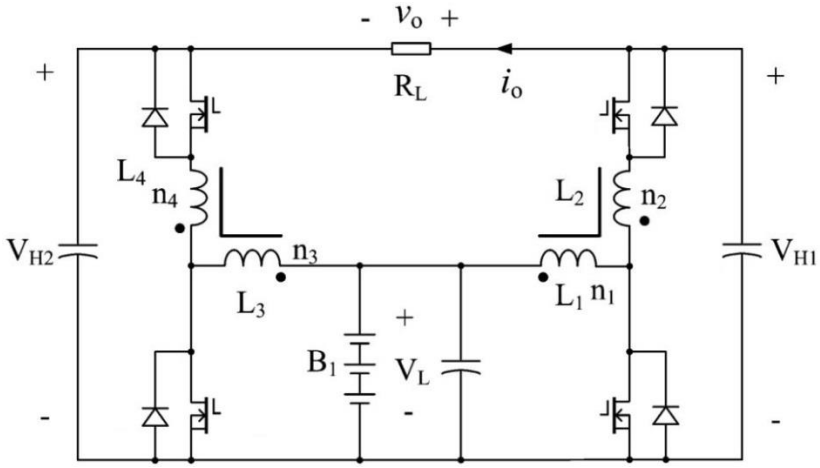

Figure 2.11: Topology of CIDBI [44]

The next type of micro-inverter is represented in Figure 2.12 as the Multilevel Energy Buffer (MEB) [45]. The MEB is connected in cascade between the input capacitor and a DC/AC converter block. The MEB consists of a Switched-Capacitor Energy Buffer (SCEB) and uses an optional Charge Control Circuit (CCC). The SCEB is used to modulate the DC/AC converter block's input voltage, functioning as an active energy buffer to reduce the total energy storage requirement. The optional CCC provides an additional means to balance the total charge entering and leaving the SCEB over a line cycle. The DC/AC converter stage is operated above the resonant frequency to achieve zero-voltage switching (ZVS) operation of 300kHz. This design can help the efficiency improve to more than 98%.

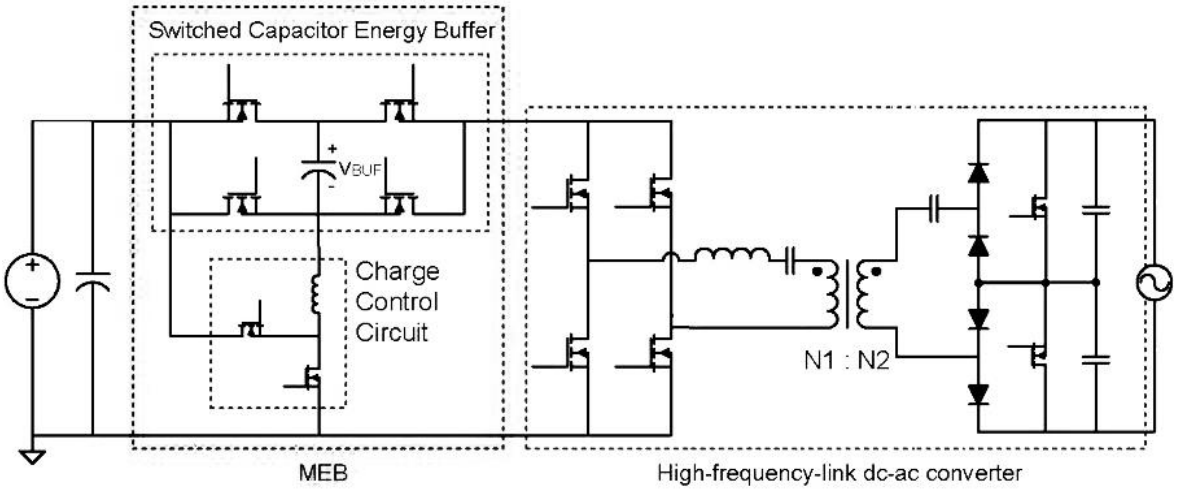

Figure 2.12: MEB micro-inverter [45]

The topology in Figure 2.13 shows the full bridge LLC inverter [46]. Its overall efficiency is 96% and it is able to provide reactive power to the grid.

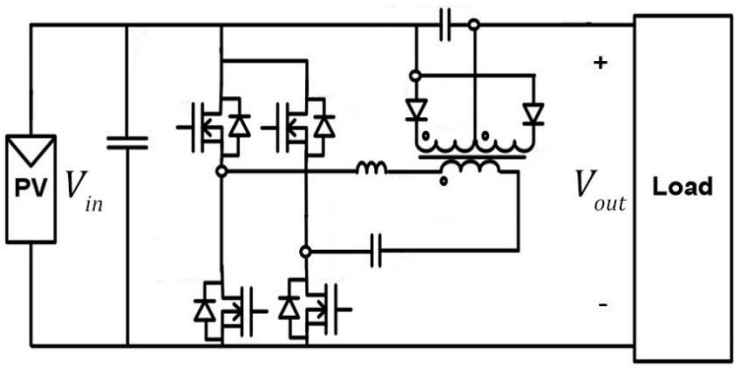

Figure 2.13: H-bridge LLC topology [46]

The topology in Figure 2.14 is the series resonant inverter using soft-switching controlling [47]. This micro-inverter comprises two active bridges, a series resonant tank and a high

frequency transformer. This system can help by reducing the component quantity number based on single-stage conversion. It also lowers the power losses due to the operation of soft-switching. Moreover, because it uses high frequency, the circuit can be reduced in size. The frequency used for this application is 100kHz with ZVS.

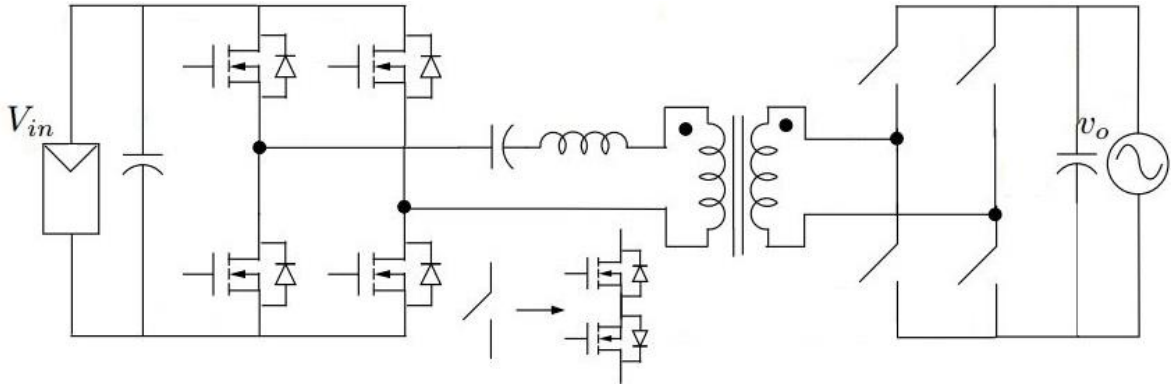

Figure 2.14: Single-stage Isolated High-frequency link Series Resonant Inverter [47]

In conclusion, the soft-switching technique to achieve the ZCS in very high frequency switching shows many advantages. This method can help lower the losses in the switches and reduce the size of components, especially the sizes of inductors and transformer. However, in this research, the switching frequency is not taken too high because of difficulties in design of MOSFET gate-drivers and control. Therefore, the soft-switching operation is not applied in this project.

The single-stage micro-inverter is a good way to for PV applications because of its simplicity. Nevertheless, in the 2-stage inverter, the control is easier than the single-stage. Moreover, the MPPT algorithms can be tested separately in the DC/DC converter without connecting to the grid or affecting the other. Therefore, in this research, the 2-stage micro-inverter is chosen.

2.4. Distribution code and grid-connection requirements

To connect to the grid, the understanding the grid requirement is needed. The following is the summary of standards and requirements for the grid connection in low voltage level. The information is mainly taken from the Distribution Code [48] of ESB Group which is the licensed operators of the electricity distribution system in the Republic of Ireland.

2.4.1. Grid standard

The first quality of the inverter is to generate an AC which meets all standards of a distribution network.

Harmonic

The fundamental voltage component U_1 is the root-mean-square (RMS) voltage value at nominal frequency of 50Hz. The individual of n^{th} order component U_n is the RMS voltage value at the frequency of n×50Hz. The individual harmonic distortion of n^{th} order is calculated as the RMS value of n^{th} order component to the fundamental RMS voltage component or U_n/U_1. The detail values of harmonic distortions are specified as in Table 2.2 below.

Harmonic Order (n^{th})	Maximum % Harmonic Distortion $\left(\frac{U_n}{U_1} \times 100\%\right)$
2^{nd}	0.70
3^{rd}	0.75
4^{th}	0.70
5^{th}	2.00
6^{th}	0.50
7^{th}	2.00
8^{th}	0.50
9^{th}	0.50
10^{th}	0.50
11^{th}	1.50
12^{th}	0.50
13^{th}	1.50
14^{th}	0.50
15^{th}	0.50
16^{th}	0.75
17^{th}	0.75
18^{th}	0.50
19^{th}	1.00

Table 2.2: Harmonic voltage distortion for individual orders

Moreover, the total harmonic distortion (THD) of all individual harmonic orders is calculated as:

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{40} U_n^2}}{U_1} \tag{2.3}$$

As the grid requirement, the total harmonic distortions THD should not exceed 5% as required in IEEE 519-1992 standard.

Frequency

The nominal grid frequency value is 50Hz. For a normal operating, the grid frequency is ranged from 49.8Hz to 50.2Hz.

Voltage

For a distribution network with low voltage, the nominal value of phase-to-phase voltage is 400VAC and the value of phase-to-neutral is 230VAC. The tolerance of the voltage is +/- 10%, so that the allowed highest phase-to-neutral voltage is 253VAC and the lowest is 207VAC.

2.4.2. Grid-connection requirements

Connection to the grid needs to follow requirements

Power factor

The power factor of the grid is defined as the ratio between the real/active power P to the apparent power S or P/S. As required, the power factor of the connection point for exporting electricity should be in between 0.95 lagging to 1. The lagging power factor means that the reactive power Q is absorbed by the generator.

The Customer shall take all reasonable steps to operate the Plant and the facility to keep the power factor of the total load at the Connection Point for exported electricity between 0.95 lagging and unity. For the purpose of this code, lagging power factor refers to the absorption of Reactive Power.

Equipment insulation

The inverter which is connected to the grid should have the insulation to withstand voltage of 3kVAC.

Islanding mode

There are two modes for a grid-connected inverter. The first one is the synchronized mode in which the inverter is connected to the distribution system. The second one is the islanding mode in which the inverter works without connecting to the grid. This happens when the distribution system is damaged or there are some emergency conditions. The inverter needs to be able to switch between the two modes during the operation.

In islanding mode, the inverter does not need to stop and it works to supply power to a local load. In designing a grid-connected inverter, there should be a relay switch between

the inverter's output and the grid. This relay has function to connect or disconnect the inverter to the grid, and to help the inverter exchange between the two modes. A voltage sensor is installed in the output of the inverter. This sensor continuously measures the grid voltage for both synchronizing and detecting unusual conditions. If the grid is lost, the relay will be turned off and the controller will change to islanding mode. In islanding mode, the inverter just supplies power to the local load and the output power of the inverter depends on the load. Voltage and frequency values are stored in the microcontroller.

In this chapter, many types of DC/DC and DC/AC converters were presented. The criteria for selecting the suitable topology for the research were also mentioned briefly. The next chapter is the presentation of the design of DC/DC converter circuit. Also, in the following chapter, the MPPT methods are tested in this DC/DC converter.

CHAPTER 3. DC/DC CIRCUIT DESIGN

The detailed analyzing, design and implementation of the selected DC/DC converter is presented in this chapter. The novel MPPT method is also described and simulated for verification. Then, the MPPT algorithms are tested in the constructed DC/DC circuit for experimental results.

3.1. Theory

3.1.1. DC/DC converter

In this section, a DC/DC converter is analyzed. As discussion on section 2.1, the SEPIC circuit is chosen because it is a buck-boost converter with non-inverting voltage and continuous input current. SEPIC stands for Single-Ended Primary-Inductor Converter, which is mentioned in many textbooks and papers [49][50][51]. However, the detail and complete analysis of this circuit cannot be found in those materials. Therefore, in this part, the formulas were developed from basic theory. In addition, there was a complete illustration of current and voltage waveforms of all components in the circuit.

The topology of SEPIC is developed from the Boost and Cuk converters. In the Cuk converter, the output inductor is used for filtering high ripples of the diode. By interchanging the diode and output inductor of Cuk converter, the SEPIC is realized. This makes the output inductor of Cuk converter to change from a filter to a part of the switching circuit and makes the output voltage to have the same polarity with the input. SEPIC is also called by an unofficial interpretation of Secondary-Polarity-Inverted-Cuk for its original development from Cuk converter with no polarity reversal.

The schematic of the SEPIC consists of two inductors and a bipolar capacitor in between. This series capacitor, which is used for energy transfer, gives protection between the input and output voltages when the switch is turned off. A diode, which is placed at the end of the converter, prevents reverse current from the output feeding back.

Operation:

When the switch is closed, the diode is reverse biased and turns off. The inductors L_1 and L_2 are charged by the input source V_I and the capacitor C_1, respectively. So that the energy is stored in both inductors and the output capacitor C_2 supplies the load current.

When the switch is opened, the current of L_1 flows through capacitor C_1, diode and into the output capacitor C_2. Both C_1 and C_2 are charged to store energy. The energy in inductor L_2 supplies to the capacitor C_2 and the output load.

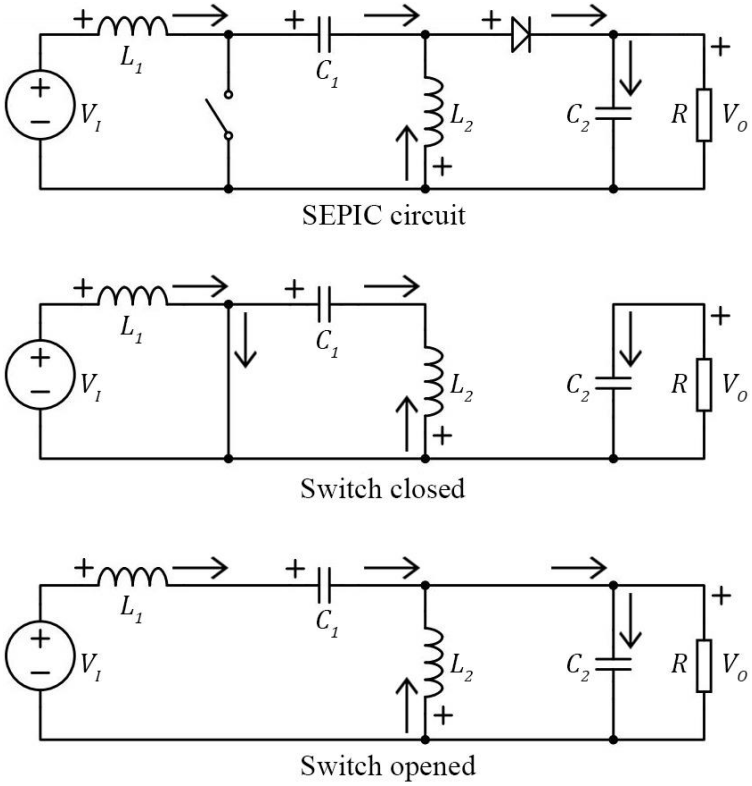

Figure 3.1: Schematic of SEPIC circuit

Initial assumptions:

The operation of the circuit is observed when the switch is closed for the time of DT and is opened for $(1-D)T$, where $f = 1/T$ is the switching frequency and D is the duty cycle. The circuit was analyzed with the following assumptions. First, the switch and diode are ideal which means there is no voltage drop when the diode and switch conduct. Second, the inductance values are large so that the currents in the inductors remain constant at their average values.

$$I_{L_{1\_open}} = I_{L_{1\_close}} = I_{L_1} \tag{3.1}$$

and

$$I_{L_{2\_open}} = I_{L_{2\_close}} = I_{L_2} \tag{3.2}$$

Third, the capacitances are large so that the voltages in the capacitors remain constant at their average values.

$$V_{C_{1\_open}} = V_{C_{1\_close}} = V_{C_1} \tag{3.3}$$

and

$$V_{C_{2\_open}} = V_{C_{2\_close}} = V_{C_2} \tag{3.4}$$

Finally, the circuit is investigated in steady-state which means the current and voltage waveforms are periodic. Hence, the average voltages across the inductors are zero for periodic operations.

$$i_L(t+T) = i_L(t) \tag{3.5}$$

then $$V_L = \frac{1}{T}\int_t^{t+T} v_L(\tau)\, d\tau = 0 \tag{3.6}$$

or $$V_{L_1} = V_{L_2} = 0 \tag{3.7}$$

In addition, the average currents in capacitors are zero for periodic voltage.

$$v_C(t+T) = v_C(t) \tag{3.8}$$

then $$I_C = \frac{1}{T}\int_t^{t+T} i_C(\tau)\, d\tau = 0 \tag{3.9}$$

or $$I_{C_1} = I_{C_2} = 0 \tag{3.10}$$

General voltage and current equations:

Using Kirchhoff's voltage law of the circuit:

$$v_I = v_{L_1} + v_{C_1} - v_{L_2} \tag{3.11}$$

After that, the Kirchhoff's current law is used:

$$i_{L_2} = i_D - i_{C_1} \tag{3.12}$$

and $$i_D = i_{C_2} + i_O \tag{3.13}$$

then $$i_{L_2} = i_{C_2} + i_O - i_{C_1} \tag{3.14}$$

Taking the average values for a period from equation (3.11):

$$V_I = 0 + V_{C_1} - 0 \tag{3.15}$$

so $$V_{C_1} = V_I \tag{3.16}$$

When the switch is closed, the voltage of inductor L_1 is equal to the input voltage:

$$V_{L_{1\_close}} = V_I \tag{3.17}$$

Taking the average values of voltages from equations (3.11) when the switch is opened:

$$V_I = V_{L_{1\_open}} + V_{C_1} + V_O \tag{3.18}$$

From equation (3.16), the equation (3.18) becomes:

$$V_I = V_{L_{1\_open}} + V_I + V_O \tag{3.19}$$

then $$V_{L_{1\_open}} = -V_O \tag{3.20}$$

For periodic operation, the voltage of inductor L_1 is zero so:

$$\left(V_{L_{1\_close}}\right)DT + \left(V_{L_{1\_open}}\right)(1-D)T = 0 \tag{3.21}$$

or $$V_I DT - V_O(1-D)T = 0 \tag{3.22}$$

then $$V_O = V_I \frac{D}{1-D} \tag{3.23}$$

Thus, the output and input voltages are related by the duty cycle. The next step is to calculate the ripple of currents and voltages on inductors and capacitors.

Current ripples of inductors:

When switch is closed, the relation between the current variation and voltage of L_1 is:

$$V_{L_1\_close} = L_1 \frac{di_{L_1}}{dt} = L_1 \frac{\Delta i_{L_1}}{\Delta t} = L_1 \frac{\Delta i_{L_1}}{DT} \tag{3.24}$$

From equation (3.17), the current ripple of L_1 then calculated:

$$\Delta i_{L_1} = \frac{V_I D}{L_1 f} \tag{3.25}$$

Similarly, the relation between the current variation and voltage of L_2 when switch is closed is:

$$V_{L_2\_close} = L_2 \frac{di_{L_2}}{dt} = L_2 \frac{\Delta i_{L_2}}{\Delta t} = L_2 \frac{\Delta i_{L_2}}{DT} \tag{3.26}$$

When the switch is closed, the voltages of L_2 and C_1 are equal together. From equation (3.16), then:

$$V_{L_2\_close} = V_{C_1\_close} = V_I \tag{3.27}$$

The current ripple of L_2 is then calculated:

$$\Delta i_{L_2} = \frac{V_I D}{L_2 f} \tag{3.28}$$

Voltage ripples of capacitors:

Taking the average values from equation (3.14) for a period:

$$I_{L_2} = 0 + I_O - 0 \tag{3.29}$$

then $$I_{L_2} = I_O \tag{3.30}$$

When switch is closed, the current of diode is zero so the average values from equations (3.12), (3.13) and (3.30) are:

$$I_{C_2\_close} = -I_O \tag{3.31}$$

and $$I_{C_1\_close} = -I_{L_2} = -I_O \tag{3.32}$$

When switch is closed, the change in charge of capacitor C_1 is:

$$\Delta Q_{C_1} = C_1 \Delta v_{C_1} = \left| I_{C_1\_close} \right| DT = I_O DT \tag{3.33}$$

then $$\Delta v_{C_1} = \frac{DI_O}{C_1 f} \tag{3.34}$$

Similar for capacitor C_2:

$$\Delta Q_{C_2} = C_2 \Delta v_{C_2} = C_2 \Delta v_O = \left| I_{C_2\_close} \right| DT = I_O DT \tag{3.35}$$

then $$\Delta v_O = \frac{DI_O}{C_2 f} \tag{3.36}$$

After calculating ripples of currents and voltages of inductors and capacitors, the conditions for the inductance and capacitance values were determined.

Continuous current condition for inductors:

For the condition of continuous current in inductor L_1, its current value should not be lower than zero.

$$I_{L_1\_min} = I_{L_1} - \frac{\Delta i_{L_1}}{2} = I_I - \frac{V_I D}{2 L_1 f} \geq 0 \tag{3.37}$$

then $$L_1 \geq \frac{V_I D}{2 I_I f} \tag{3.38}$$

The same with inductor L_2 for the continuous current condition:

$$I_{L_2\_min} = I_{L_2} - \frac{\Delta i_{L_2}}{2} = I_O - \frac{V_I D}{2 L_2 f} \geq 0 \tag{3.39}$$

then $$L_2 \geq \frac{V_O D}{2 I_O f} \tag{3.40}$$

Continuous voltage condition for capacitors:

The continuous voltage condition for the capacitor C_1 is that the minimum voltage value should not be lower than zero.

$$V_{C_1\_min} = V_{C_1} - \frac{\Delta v_{C_1}}{2} = V_I - \frac{DI_O}{2 C_1 f} \geq 0 \tag{3.41}$$

$$C_1 \geq \frac{DI_O}{2 V_I f} \tag{3.42}$$

Similar for the capacitor C_2 of the continuous voltage condition:

$$V_{C_2\_min} = V_{C_2} - \frac{\Delta v_{C_2}}{2} = V_O - \frac{DI_O}{2 C_2 f} \geq 0 \tag{3.43}$$

$$C_2 \geq \frac{DI_O}{2 V_O f} \tag{3.44}$$

Hence, conditions for values of inductors and capacitors are shown above. They are the base for choosing suitable values of SEPIC components.

Relation of input voltage and current when the output is connected to a resistor:

The case of the SEPIC output is connected to a resistor R is considered for the simulation and experiment in sections 3.3 and 3.6. Assume that there is no loss of the SEPIC circuit, the input and output power will be the same:

$$V_I I_I = P_{in} = P_{out} = V_O^2/R \tag{3.45}$$

From the equation (3.23), it is then:

$$\frac{V_I}{I_I} = \left(\frac{1}{D} - 1\right)^2 R \tag{3.46}$$

Hence, the relation of the input voltage and input current is controlled on the duty cycle D of the switch. The relationship the input voltage and current to the duty cycle and resistor is illustrated in Figure 3.4.

To sum up, average values on one period, the time of switch closed and the time of switch opened are shown in the following Table 3.1. Also, the theoretical voltage and current waveforms of SEPIC components are illustrated in Figure 3.2 and Figure 3.3.

	Period T	Switch closed DT	Switch opened $(1-D)T$
V_{SW}		0	$V_I + V_O$
I_{SW}		$I_I + I_O$	0
V_{L_1}	0	V_I	$-V_O$
I_{L_1}	I_I	I_I	I_I
V_{L_2}	0	V_I	$-V_O$
I_{L_2}	I_O	I_O	I_O
V_{C_1}	V_I	V_I	V_I
I_{C_1}	0	$-I_O$	I_I
V_{C_2}	V_O	V_O	V_O
I_{C_2}	0	$-I_O$	I_I
V_D		$-(V_I + V_O)$	0
I_D		0	$I_I + I_O$

Table 3.1: Average voltage and current values of SEPIC components

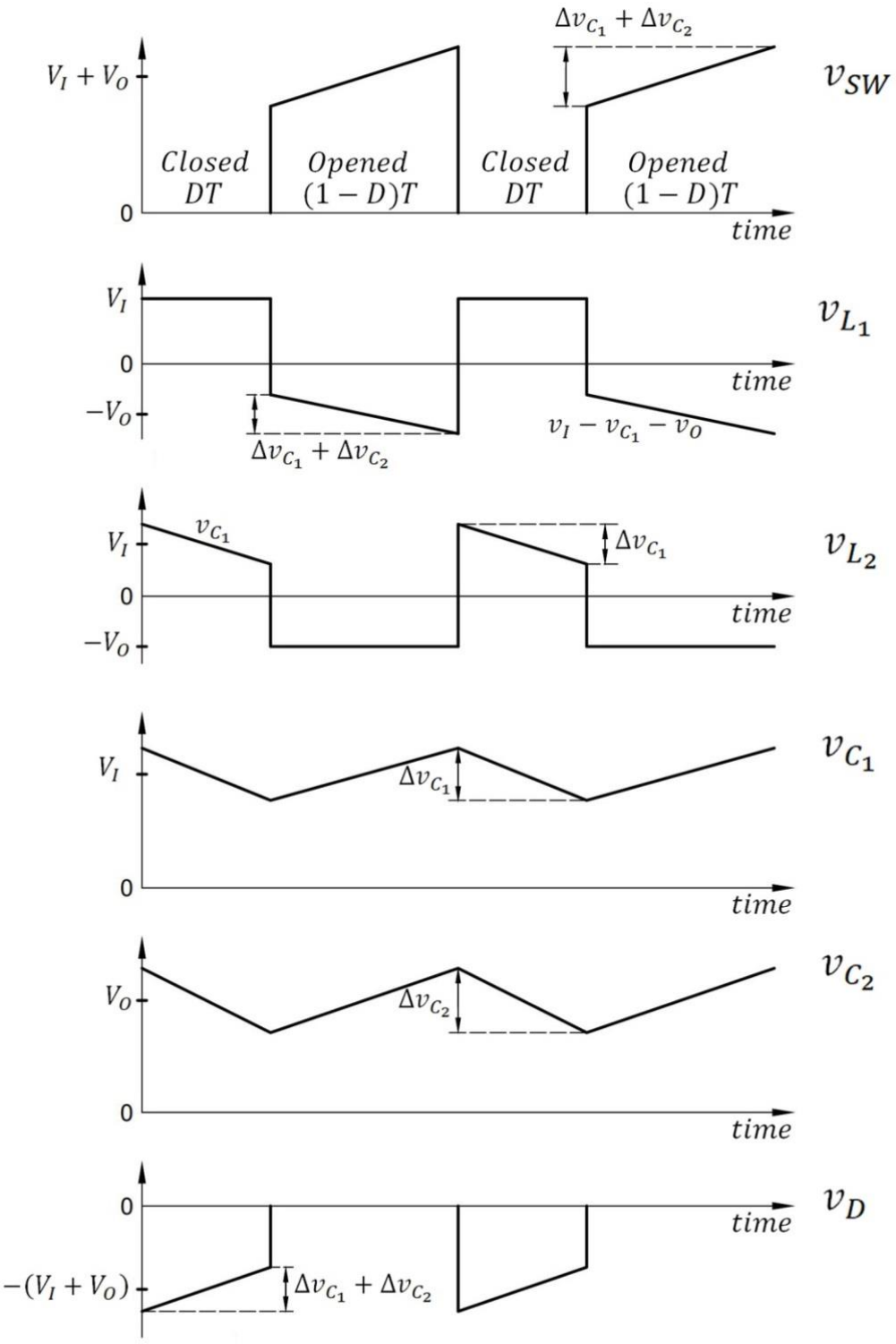

Figure 3.2: Voltage waveforms of components of SEPIC circuit

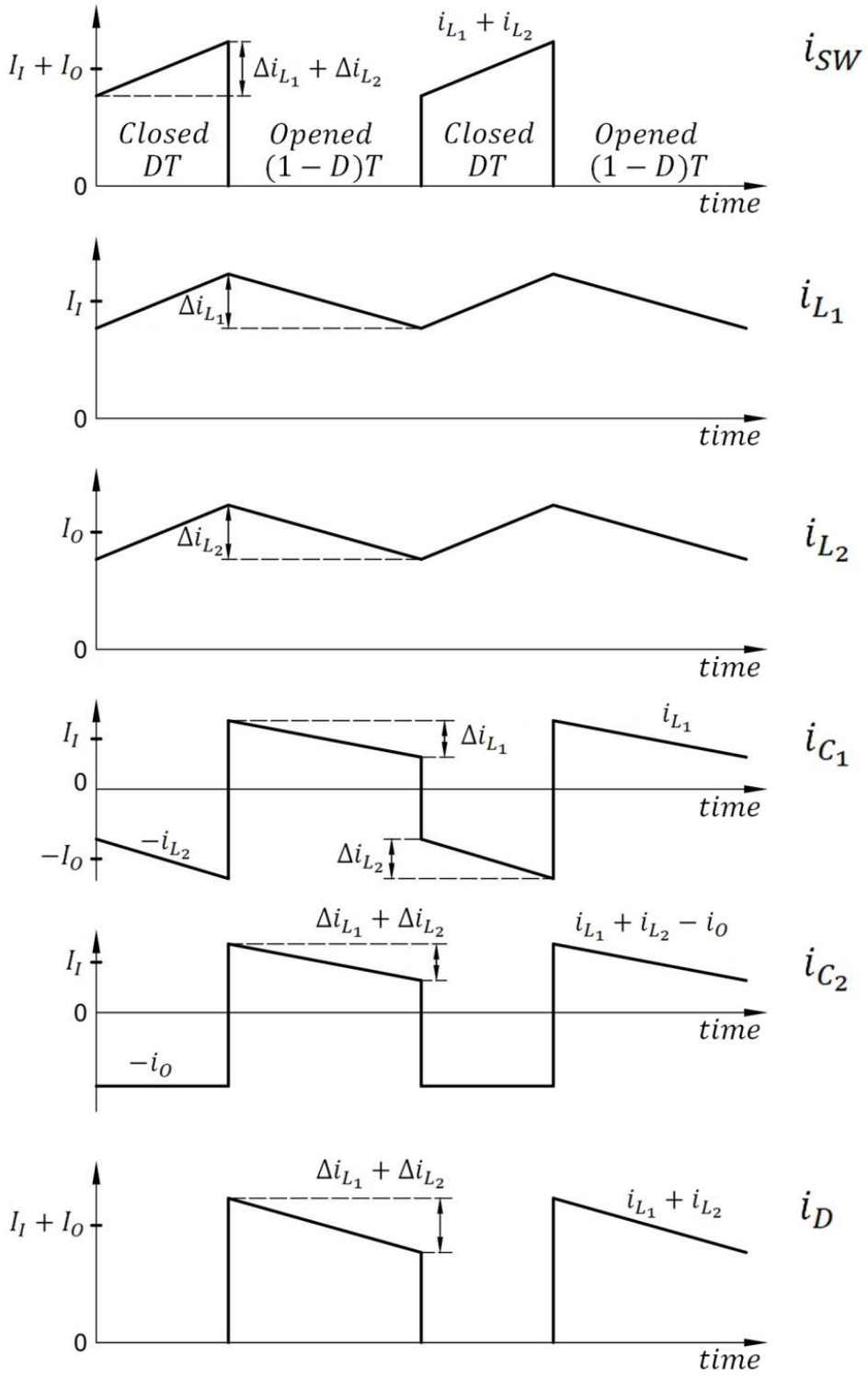

Figure 3.3: Current waveforms of components of SEPIC circuit

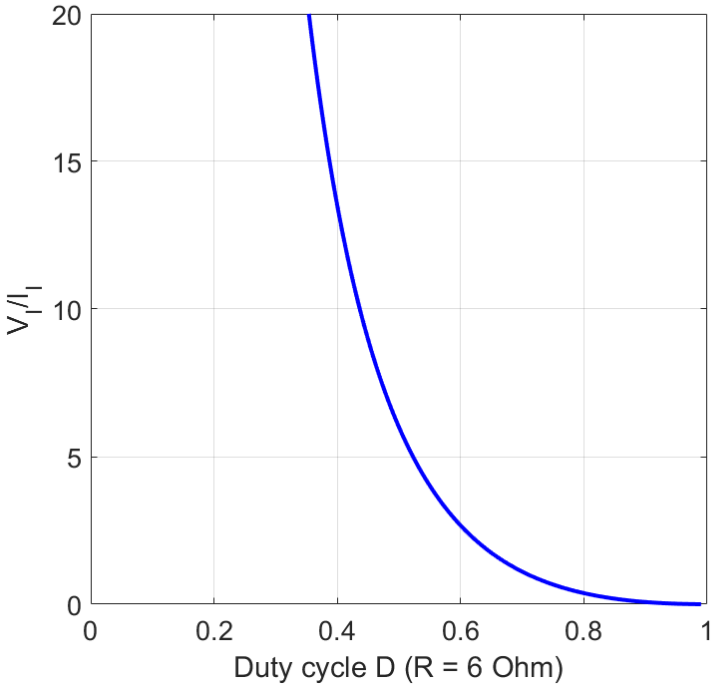

Figure 3.4: Relation of SEPIC input voltage and current with output resistor

3.1.2. MPPT algorithm

In this part, the modified MPPT method of P&O is described and studied for comparison purpose. The operating power point using the original version of this algorithm can only oscillate at the vicinity of MPP, meaning it cannot get to the exact MPP. Therefore, a modified P&O method is developed, being able to keep power point not fluctuating when it gets close to MPP. This modified P&O method is then similar to the traditional INC, which keeps the PV voltage at certain points near the MPP. By combining the traditional P&O and binary-search technique, a novel algorithm that performs at high precision with fast convergence time is demonstrated. This technique is easy to build and simple to control. The flowcharts of these MPPT methods under consideration are presented in the next sections.

3.1.2.1. Modified Perturb & Observe method

As mentioned in section 2.2.1, the traditional P&O method is simple but it makes the operating power point of solar panel fluctuate around the MPP and can lead to power loss by the oscillatory effect; this would be seen in the simulation section 3.3. In the modified P&O, a stop condition is added for preventing the oscillation. When the absolute value of power variation ΔP is less than an amount of ε_{PO}, which means that the operating power

point is near the MPP and the converter should remain at this operating point. Changes of temperature and/or irradiation which cause large variation in power ($|\Delta P| \geq \varepsilon_{PO}$) will make the system to search for a new optimum operating point. The flowchart of the modified P&O method is shown in Figure 3.5.

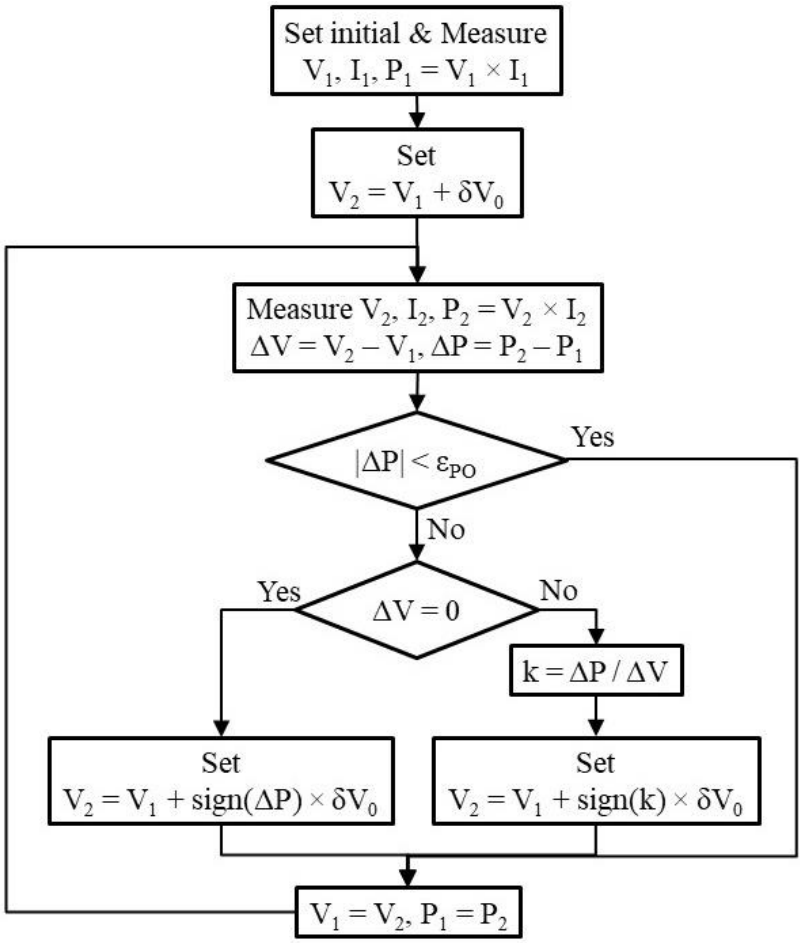

Figure 3.5: Flowchart of Modified P&O method

In the beginning, the DC/DC converter is set to the initial PV voltage of V_1. Then the panel voltage is set higher than the previous one by an amount of δV_0. The PV voltage and current are measured to determine ΔP and ΔV. In the case that the absolute value of ΔP is smaller than ε_{PO}, the converter is unchanged. In other circumstances, the PV voltage is added or subtracted by an amount of δV_0 to track to the MPP. In case of ΔV equals to zero, the value of $\Delta P/\Delta V$ is incalculable so that the two cases of ΔP and $\Delta P/\Delta V$ are considered. The values of ΔP and $\Delta P/\Delta V$ are negative when the operating point is on the right side of MPP and vice versa. Therefore, the signs of ΔP and $\Delta P/\Delta V$ can be used to determine the required change of the panel voltage for better power extraction from the PV.

To improve the efficiency of this method, a variable δV is proposed at different stages of the MPPT. For tracking MPP, δV should have a large value to quickly reach near the MPP. For maintaining MPP, δV will be reduced to get as close as possible to MPP. Therefore, a novel and simple method to achieve all the conditions above is introduced in the following section.

3.1.2.2. Binary-search-based Perturb & Observe method

The bisection search theorem (BST) applied for MPPT is presented in [52][53], where the searching scans in large range of panel voltage from zero to V_{OC}. With any changes in irradiation or temperature the algorithm starts from the beginning. This reduces the efficiency and causes power loss.

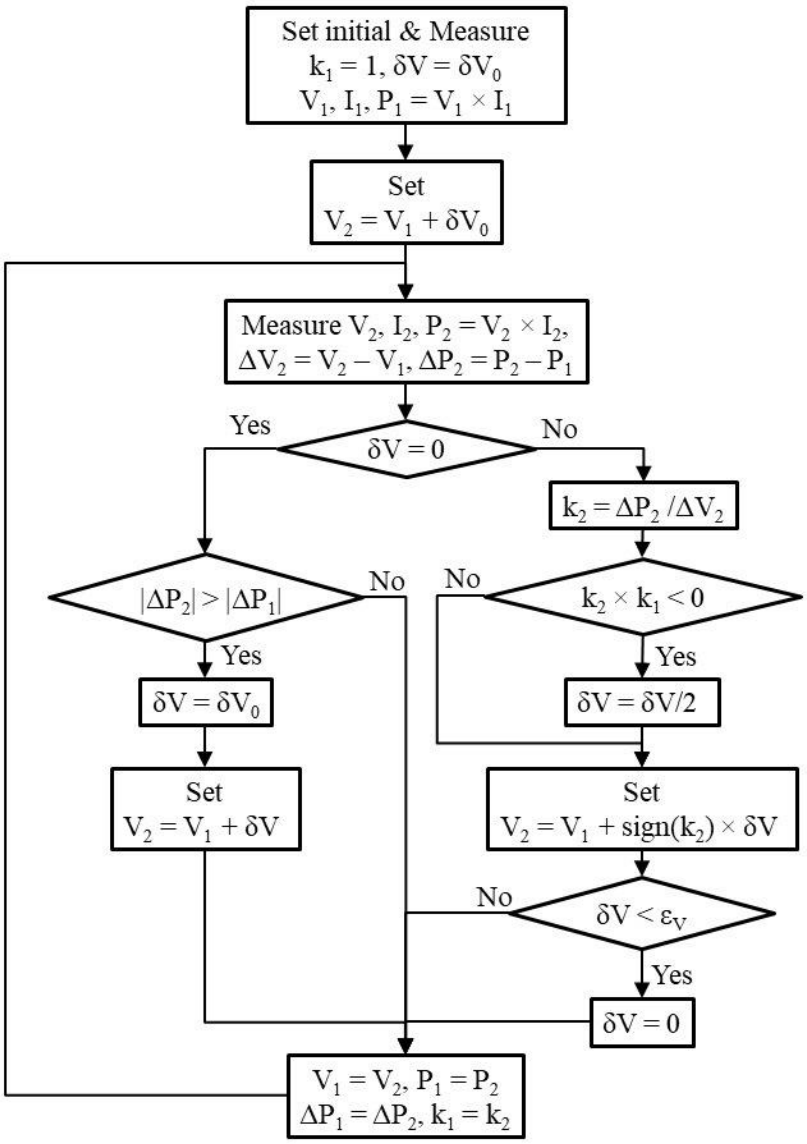

Figure 3.6: Flowchart of BS-P&O method

The novel binary-search-based P&O (BS-P&O) algorithm introduces the variable step of finding the MPP. The algorithm of this MPPT is shown in Figure 3.6.

In the beginning, a large δV is used for quickly tracking to near MPP. It is known that ΔP/ΔV is negative when the operating point is at the right side of MPP and vice versa. Therefore, every time the value ΔP/ΔV changes its sign, the MPP must be between the two latest operating points. Thus, the change of voltage δV will be divided by 2 when approaching closer to the exact MPP. This simple method helps reach close to MPP with an exponential convergence rate. The operation of this method can be easier understood by the illustration in Figure 3.7.

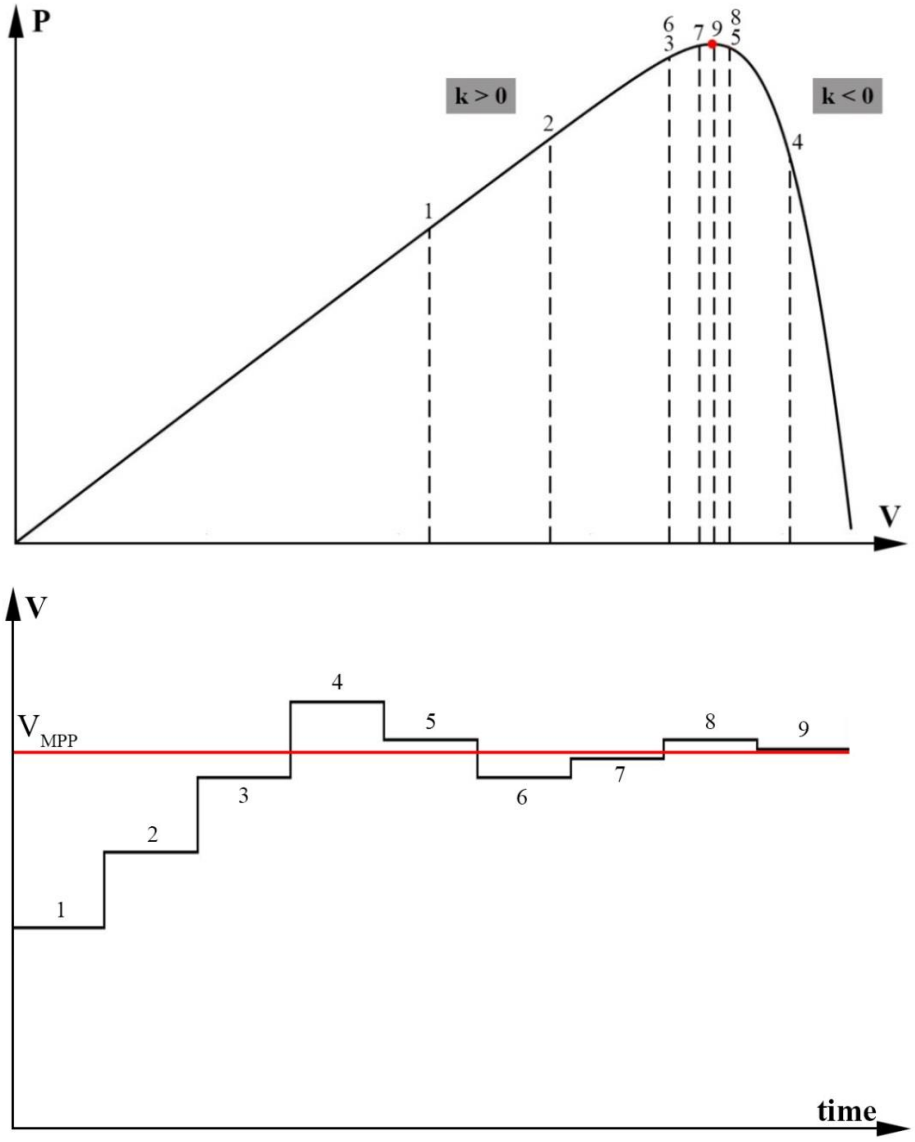

Figure 3.7: Illustration of BS-P&O method

When δV equals zero, if there is any change of environment making the value of ΔP larger than the previous one, the algorithm will immediately set δV to δV_0 and start to search for the next MPP. When the δV becomes too small and less than ε_V, the value of δV is set zero.

3.2. Refinement of MPPT algorithms

In the simulation and the programming, the voltage of the solar panel is set by duty cycle of the converter. The absolute and precise values of measured voltage and current cannot be achieved in practice because there is always noise and measurement errors, which affect the measured results. Therefore, the flowcharts of the MPPT methods need to be adjusted to suit the control of the microcontroller in practice. The SEPIC circuit is selected for the DC/DC converter, so that the duty cycle D is the controlling signal of this circuit.

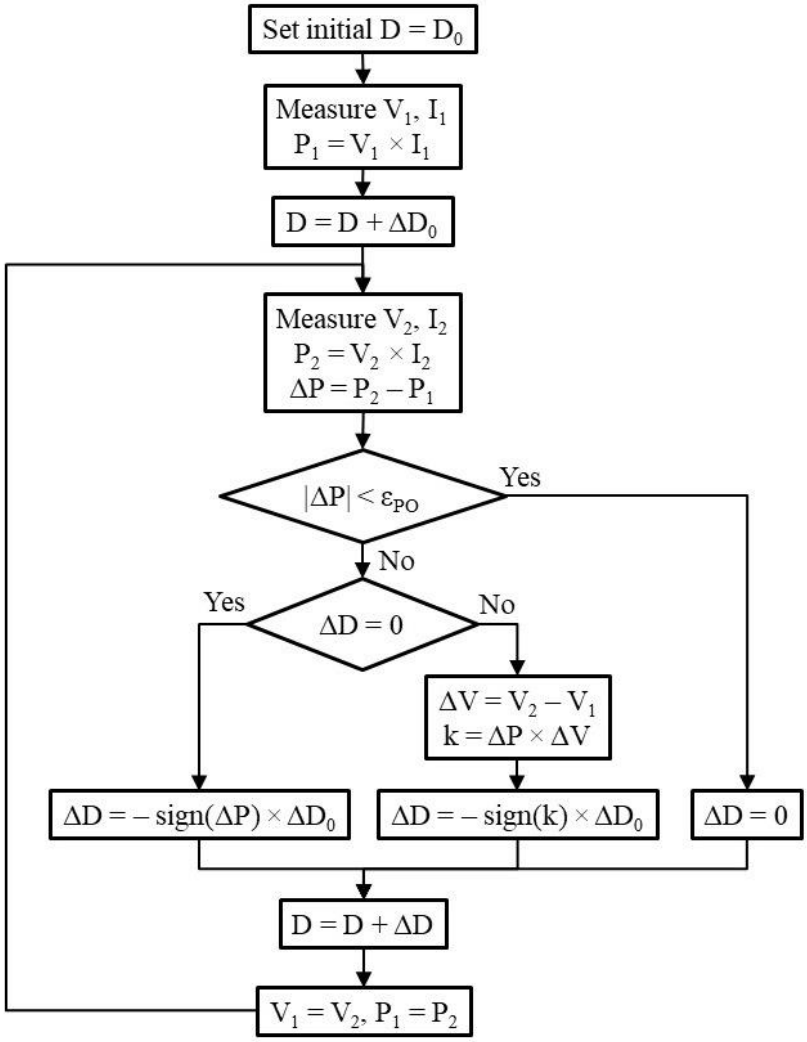

Figure 3.8: Flowchart of Modified P&O in simulation and programming

The flowchart in Figure 3.8 is based on Figure 3.5. In the beginning, the duty cycle D is set to D_0 and the initial panel voltage and current are measured. Then the panel voltage is controlled by adding or subtracting to the duty cycle D an amount of ΔD_0. The detailed description is already mentioned in the previous section.

The flowchart in Figure 3.9 is an adaptable version of Figure 2.7. The parameter ε_I and ε_{INC} are added to the flowchart because it is impossible to have zero values of ΔI and k in practical measurement.

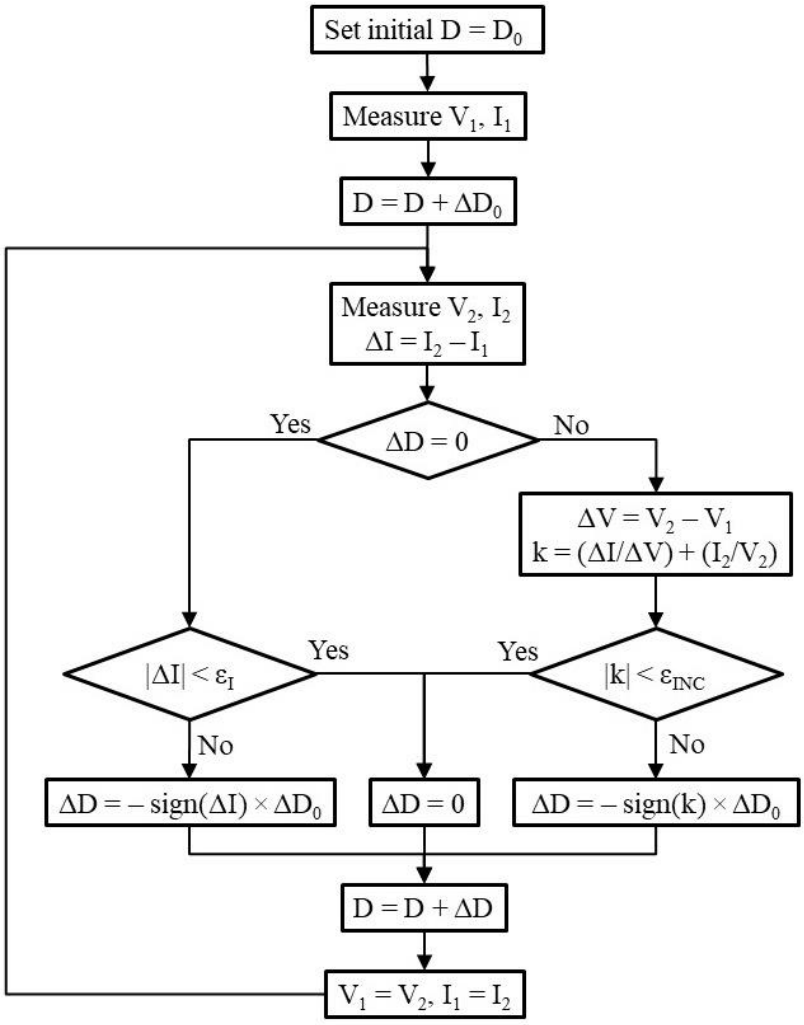

Figure 3.9: Flowchart of INC in simulation and programming

Similarly, the flowchart in Figure 3.10 is modified from the one in Figure 3.6. The value of ε_P is added to compensate for unwanted fluctuation of the measurement. Instead of ε_V, the parameter ε_D is used as a limit for the program to stop dividing ΔD as it becomes too small. The signs of k_1 and k_2 are used to determine the direction of the duty cycle. The value of

them is not necessary, therefore k_2 is calculated as the product of ΔP_2 and ΔV_2. This avoids having large values for k_2 when ΔV_2 is small.

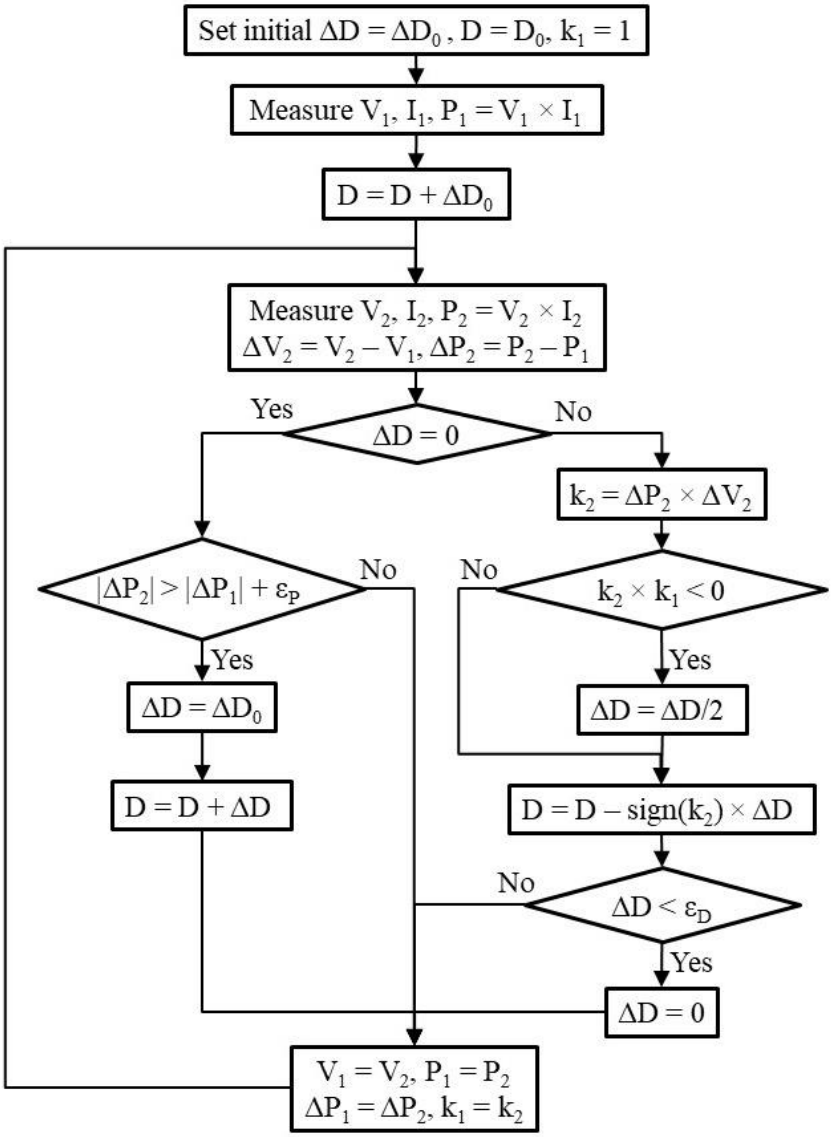

Figure 3.10: Flowchart of BS-P&O in simulation and programming

Hence, the three MPPT algorithms of modified P&O, INC and BS-P&O in Figure 3.5, Figure 2.7 and Figure 3.6 are refined to suit the practical approach in Figure 3.8, Figure 3.9 and Figure 3.10 respectively. These flowcharts are applied and simulated in the next section.

3.3. Simulation

The simulation model is built on MATLAB/Simulink. A SEPIC is used for testing the performance of MPPT algorithm. Its output is connected to a resistor R. A capacitor C_3 is put between the PV panel and the SEPIC to reduce drastic change and oscillation of the panel voltage.

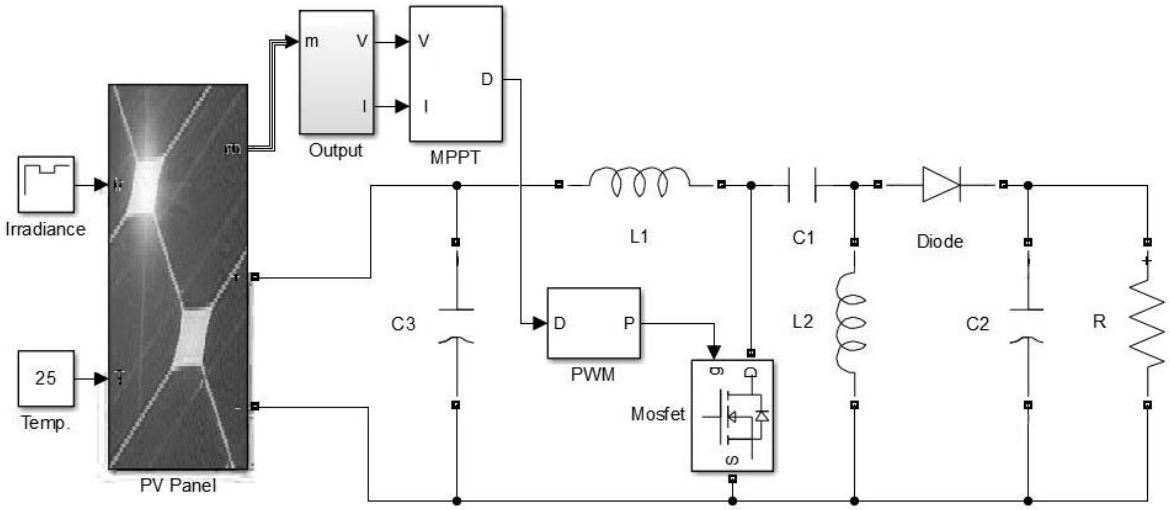

Figure 3.11: MATLAB simulation model for MPPT verification

The MOSFET switch is driven by a PWM block, which operates at the frequency of f_{sw}. The duty cycle for controlling the switch is updated at the sampling period of T_s. Component values of the SEPIC circuit are listed in Table 3.2.

$C_1 = 10\mu F$	$L_1 = 2mH$
$C_2 = C_3 = 1000\mu F$	$L_2 = 2mH$
$T_s = 0.02s$	$R = 5\Omega$

Table 3.2: Simulation values for SEPIC components

The solar panel used for the simulation is the Perlight Solar PLM-280P-72. The irradiance is set at 1000W/m^2 for the first 0.36s, 800W/m^2 from 0.36s to 0.72s and back to 1000W/m^2 from 0.72s to 1.08s. The temperature of the solar module is kept constant of 25°C.

$D_0 = 0.5$	$\Delta D_0 = 0.016$
$\varepsilon_{PO} = 3.5W$	$\varepsilon_I = 0.04A$
$\varepsilon_{INC} = 0.03A/V$	$\varepsilon_D = 0.001$
$\varepsilon_P = 0.5W$	$f_{sw} = 40kHz$

Table 3.3: Simulation values for MPPT parameters

In the simulation, the change of duty cycle ΔD_0 is set large enough to notice easily. In practice, it can be chosen for smaller values compared to this simulation. The values of ε_{PO}, ε_I and ε_{INC} are chosen so that the stop conditions are nearly the same for both modified P&O and INC methods.

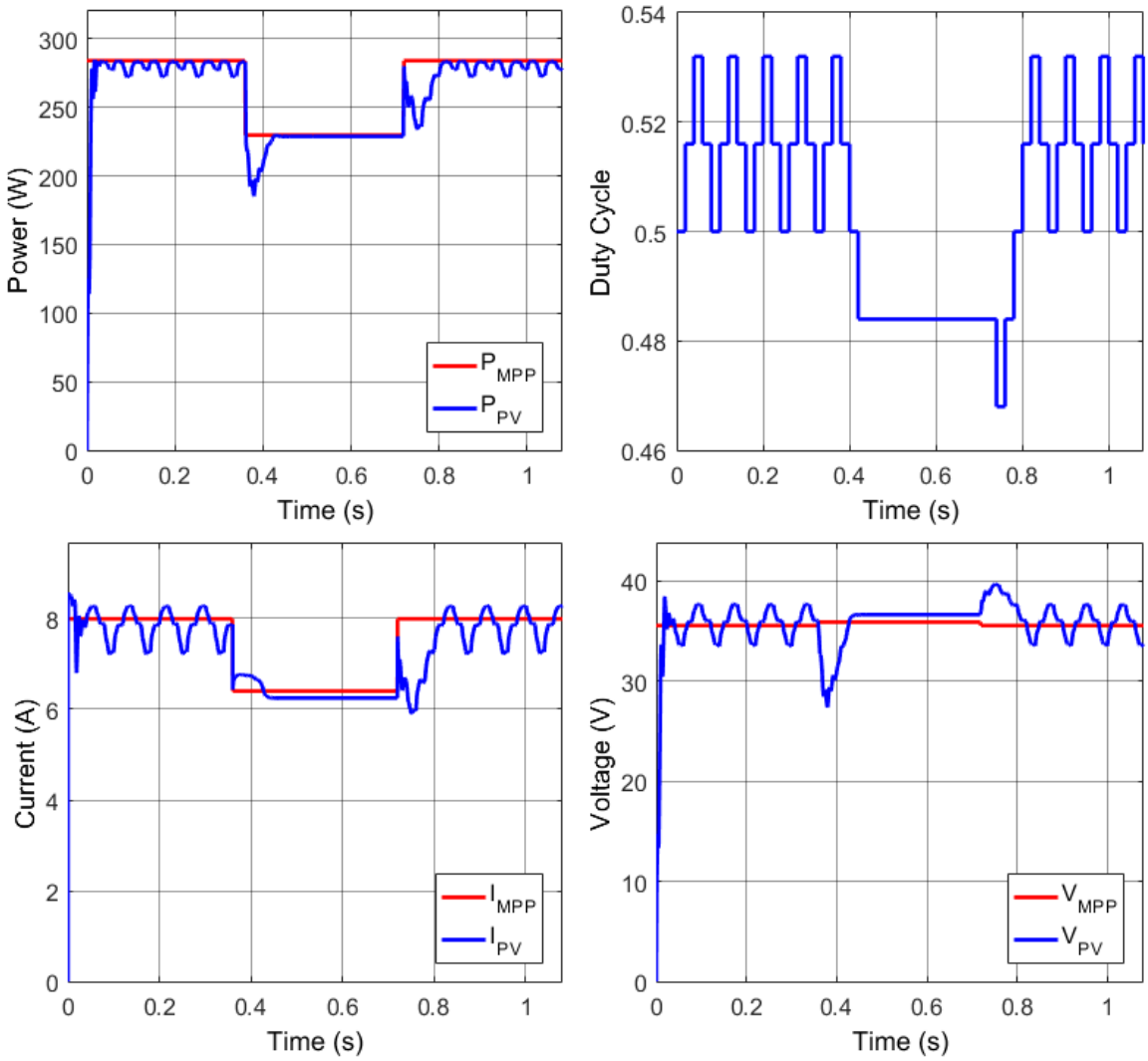

Figure 3.12: Modified P&O and INC simulation results

The simulation results of the modified P&O and traditional INC methods with set values in Table 3.3 to give similar performance are shown in Figure 3.12. At irradiance of 1000W/m^2, the operating power point P_{PV} cannot get close to P_{MPP} because of the large ΔD_0. The panel voltage V_{PV} keeps moving up and down or oscillating around the V_{MPP} and cannot settle down because the $|\Delta P|$ is larger than the ε_{PO} and the $|k|$ is larger than ε_{INC} in the modified P&O and INC respectively. In this section, the modified P&O and INC operate as the traditional P&O. At irradiance of 800W/m^2, the duty cycle keeps unchanged but the difference between the operating power point and the MPP is 1.9W. It can be

concluded that the two algorithms may not fluctuate in some certain circumstances but not for all conditions.

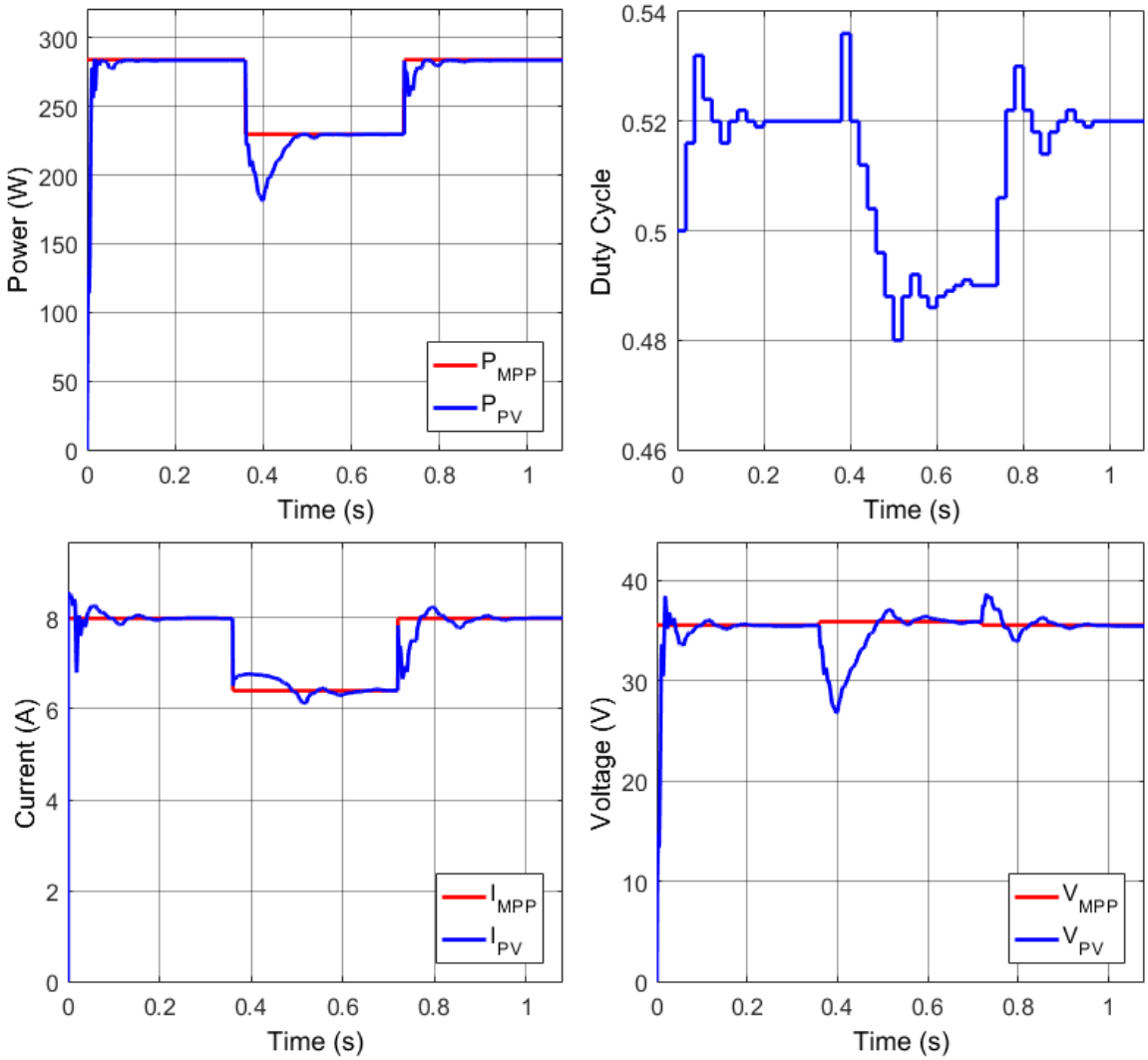

Figure 3.13: Binary-Search-Based P&O simulation results

For the BS-P&O result in Figure 3.13, the change of duty cycle ΔD is decreased exponentially from a large initial value to small values near MPP (in the simulation, ΔD declines to less than 0.001). This helps operate near the MPP with an error less than 0.05W in comparison to the theoretic MPP. The response time of the algorithm is less than 0.2s, which is quick enough for changes of the irradiance. In steady state, the efficiency in the simulation of the modified P&O and INC is 98.9% and the BS-P&O is 99.9%. Hence, through the simulation, the new BS-P&O method has been proven to perform better than the tradition INC and modified P&O methods. Moreover, the novel method has shown its effectiveness in efficiency and fast response time.

Features	Traditional P&O		Modified P&O and INC				BS-P&O
	ΔD_0 (fixed)		ΔD_0 (fixed)		ε_{PO}, ε_I, ε_{INC}		ΔD (variable)
	Large	Small	Large	Small	Large	Small	Large→Small
Accurate	×	✓	×	✓	×	✓	✓
Fast	✓	×	✓	×	-	-	✓
Not fluctuating	×	×	-	-	✓	×	✓

Table 3.4: Comparison of MPPT methods

Table 3.4 is the summary of the performance of the MPPT methods. For the traditional P&O, the operating points always fluctuate around the MPP. The step size of the traditional P&O is fixed. With a large step size, the system can respond quickly to changes of the environment but the accuracy is low. With a small step size, the system can get a high MPPT efficiency, however the response time of this method is low. Choosing either large or a small step size in the traditional P&O would lead to advantage of one feature and disadvantage of the other.

For a modified P&O and INC, the problem is the same as the traditional P&O for their fixed step size. However, there are added conditions where the operating points stop fluctuating. The stop conditions are defined by parameters ε_{PO}, ε_I and ε_{INC}. If these parameters are large, the system may stop at a point which is far from the MPP. But if the parameters are small, the operating point can stop at a point which is close to the MPP, however the noise of the measurements can make the system stop at any point. So that, the stop parameter would be very careful chosen and the measurement noise should be considered.

For the BS-P&O method, the problems of the P&O and INC are solved by applying variable step size. The step size is large in the beginning and becomes smaller when the operating point has just passed the MPP. By doing this, the method can achieve both accuracy and fast response. The stop condition occurs when the step size gets close to zero which means that the system stops fluctuate without using stop parameters as in the modified P&O and INC methods.

The experiment for these MPPT methods are carried out for verifying the theory and simulation results in section 3.6.2.

3.4. Circuit board design

The solar panel used for the experiment is monocrystalline solar module of Perlight Solar manufacturer. The detail information of this panel at Standard Test Condition (STC) is listed in Table 3.5. The STC is used to indicate the performance of solar module. A solar cell at STC has its temperature of 25°C, irradiance of 1000W/m^2 and air mass of 1.5 (AM1.5 or solar irradiation angle of 45°).

Figure 3.14: Solar module of the experiment

Manufacturer part number	PLM-280M-72
Peak power P_{max_STC}	280W
Short circuit current I_{sc_STC}	8.32A
Open circuit voltage V_{oc_STC}	44.2V
Maximum power current I_{mp_STC}	7.73A
Maximum power voltage V_{mp_STC}	35.9V
Temperature coefficient of open-circuit voltage η_{Voc}	–0.333%/°C
Temperature coefficient of power η_P	–0.459%/°C
Power tolerance	±3%

Table 3.5: Technical information of PLM-280M-72 solar module

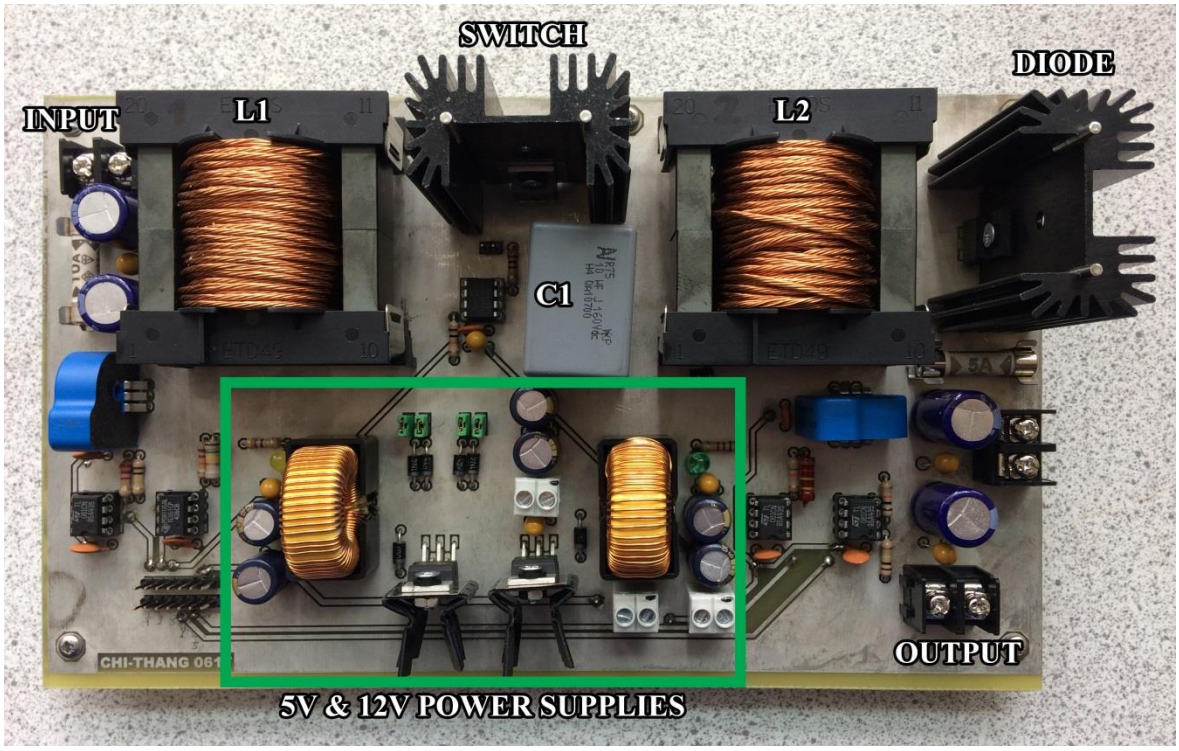

Figure 3.15: Laboratory prototype of DC/DC board

A 10A fuse is put at the input to protect the circuit from unexpected high current. The two power components, which consume most power, are the MOSFET and diode. Therefore, two heat-sinks 6399BG with the thermal resistance of 3.3°C/W are used for dissipating heat from the MOSFET and diode.

The board also includes the power supply circuit, gate driver, sensors and inductors, which will be presented in the following sections.

3.4.1. Power Supply

The circuit needs power supplies for the sensors and gate drivers of about 5W. The sensor circuits consist of op-amps and comparators that use a 5V supply. In addition, a 12V supply is used for the MOSFET gate driver circuits. These 5V and 12V power supplies will be used for both DC/DC and DC/AC boards. The estimated power of all the sensor, gate-driver and control circuits is 4W for 5V power supply and 1W for 12V supply or the output current of 0.8A for 5V supply and 0.083A for 12V supply.

The source for the power supplies can be taken from the input of the PV panel or from the battery. There are two common methods of regulating from high to low voltage.

The first way is using the linear regulators. However, the power losses are considerable. For the PV input of 35V, the power losses of these regulators are:

$$P_{loss\_5V} = (V_{in} - 5) \times I_{out} = (35 - 5) \times 0.8 = 24W \quad (3.47)$$

$$P_{loss\_12V} = (V_{in} - 12) \times I_{out} = (35 - 12) \times 0.083 = 1.9W \quad (3.48)$$

The loss of the linear regulators is large, so that the switching regulators TL2575HV-05 and TL2575HV-12 are chosen. These regulators are able to output the 1A current with the efficiency about 80%. This means the power loss of both is less than the one of linear regulators. The highest operation voltage of these regulators is 60V, which is higher than the open-circuit voltage V_{oc} of the solar module. However, extra components will be used for these ones.

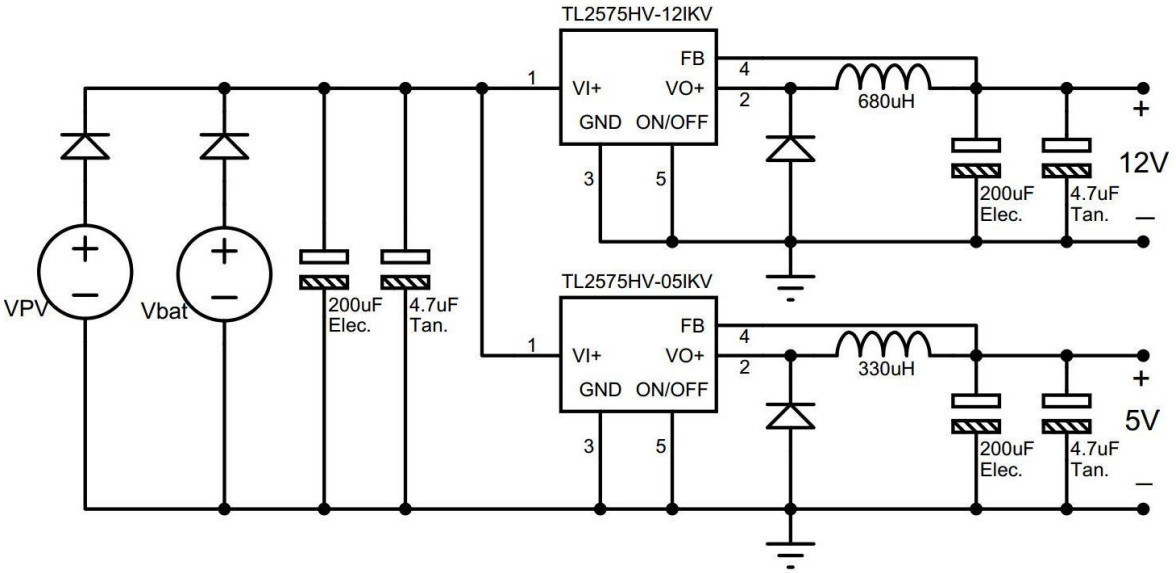

Figure 3.16: Schematic of 5V and 12V power supplies

Among the external components, two inductors of 330µH and 680µH are used. The combination of tantalum and electrolytic capacitors help stabilize voltage and reduce noise. The electrolytic capacitors with high capacitance can maintain the voltage while the tantalum is used for getting rid of noise and high frequency pulses.

There are two diodes, which are put at the output of the input sources V_{PV} and V_{bat}. The supply can be taken from both PV panel and battery. One of the two diodes will conduct when one of the two voltage levels is higher than the other. This helps to provide the source uninterruptedly at night or in shaded conditions.

3.4.2. MOSFET gate driver

To switch the MOSFET on and off with a control signal from a microcontroller, a gate driver circuit is needed. In this application, TC4428A is used for driving the MOSFET. The driver typically has the delay time of 30ns, rise time and fall time of 25ns, which is

suitable for switching frequency of the MOSFET. Moreover, TC4428A has one non-inverting and one inverting driver, which can be used for not only low-side but also high-side MOSFET driving applications.

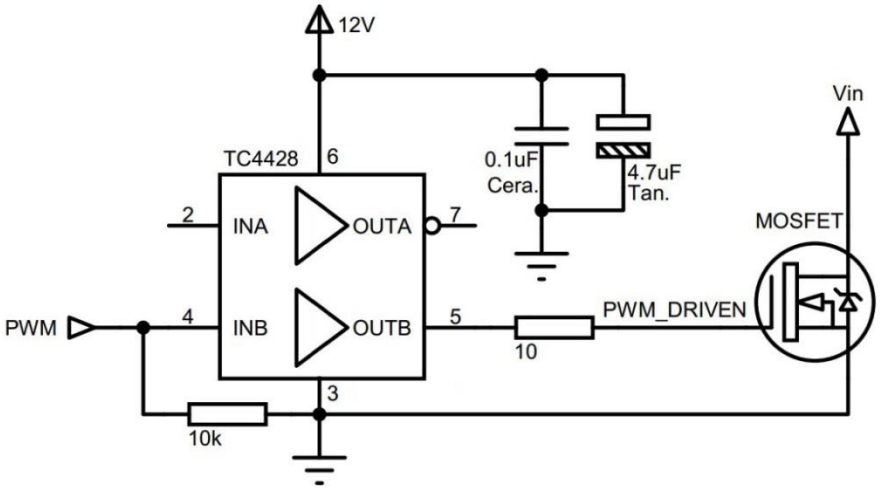

Figure 3.17: Schematic of low-side MOSFET driver

A combination of ceramic and tantalum capacitors between the power supply and ground of the driver is applied to get rid of noises caused during the switching.

3.4.3. Current sensor

There are many way of measuring current. One of the most common ways is using a resistor with a very low resistance. The resistor will be connected in series to the circuit and the current flowing through it makes a voltage drop on this resistor. This voltage value is then read by a microcontroller and the current value is measured by simply dividing the voltage drop to the resistance. The resistor needs to be small enough that it will not consume too much power from the source. However, if the value of resistor is too small, the voltage drop in it is small too and it is challenging to read the exact value of current.

Figure 3.18: Current transducer LTS 6-NP

The other way of measuring current is using the Hall Effect. This kind of current measurement is energy effective and precise. The current transducer LTS 6-NP is chosen for it has bidirectional current input and multiple ranges. Because the current can flow bi-directionally, it can be used for both DC and AC measurement. Moreover, with multiple ranges this sensor may be adjusted for different current levels. The maximum current value that can pass through it is 19.2A and the accuracy of this sensor is ±0.2% which is suitable for this application. The sensor voltage supply is 5V, which is available from the circuit. In addition, there is no external component needed.

3.4.4. Voltage sensor

The PV voltage is above 30V but the maximum input voltage for a microcontroller is 3.3V. Therefore, a simple voltage follower with an op-amp is applied.

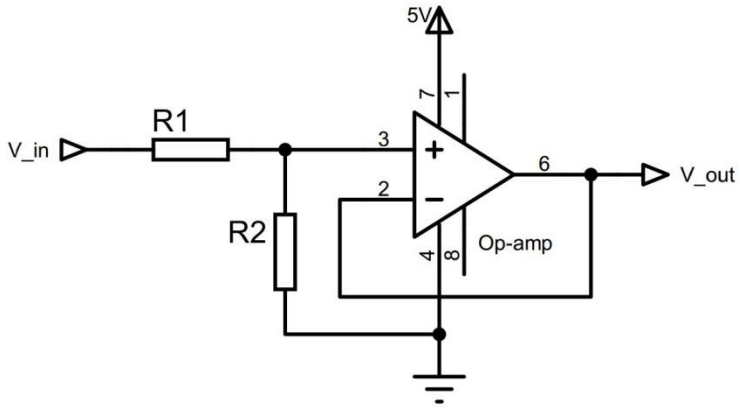

Figure 3.19: Schematic of DC voltage sensor

The input voltage is stepped down by two resistors R_1 and R_2 before coming to the op-amp. The relation of the input and output voltages is shown in the equation below.

$$\mathrm{V_{out}} = \frac{\mathrm{R_2}}{\mathrm{R_1 + R_2}}\mathrm{V_{in}} \tag{3.49}$$

In the experiment, the maximum input voltage of the solar panel at 0°C and irradiation of 1000W/m^2 is calculated as:

$$V_{oc\_0℃} = V_{\mathrm{oc}\_STC}\left(1 + \eta_{Voc}(0 - T_{STC})\right) \tag{3.50}$$

or
$$V_{oc\_0℃} = 44.2(1 + 0.00333 \times 25) = 47.9\mathrm{V} \tag{3.51}$$

The output voltage should be less than 3.3V, therefore:

$$\frac{\mathrm{R_2}}{\mathrm{R_1 + R_2}}47.9 \leq 3.3 \tag{3.52}$$

or $$\frac{R_1}{R_2} \geq 13.5 \quad (3.53)$$

Choose R_1 of 150kΩ and R_2 of 10kΩ. The ratio of R_1 to R_2 is 15 and the ratio of the input to output voltage is 16.

3.4.5. Inductor and capacitor conditions

The chosen switching frequency for the SEPIC is 40kHz. The noise is created at switching frequency by reactive components such as inductors and transformer. The human hearing frequency ranges from 20Hz to 20kHz, so that the switching frequency needs to be higher than this range to make the noise inaudible to human ears. The size of inductors is proportionally reduced when the switching frequency is increased or the higher the frequency gives a smaller inductor. Nonetheless, too high value of frequency causes difficulties in designing the MOSFET gate-drivers and control, thus 40kHz was selected for this project.

The conditions for inductance and capacitance values can be determined by the chosen switching frequency. The solar panel in the experiment has the maximum power of 280W. In the case of just 100W output is obtained, as seen in the datasheet of the solar panel, the panel voltage at MPP is about 33V, so that the output current is calculated as 3A. From the equation (3.38), the condition of L_1 is calculated as below:

$$L_1 \geq \frac{D_{max}}{2f}\left(\frac{V_I}{I_I}\right)_{max} = \frac{1}{2 \times 40000}\frac{33}{3} = 0.14\text{mH} \quad (3.54)$$

Similar to the L_1 inductor, the condition of inductor L_2 is taken from equation (3.40) as:

$$L_2 \geq \frac{D_{max}}{2f}\left(\frac{V_O}{I_O}\right)_{max} = \frac{1}{2 \times 40000}\frac{33}{3} = 0.14\text{mH} \quad (3.55)$$

The next step is the condition of capacitor C_1 from equation (3.42). The maximum input current of the solar panel is 8A, so that the output current is chosen for the case of 10A. The input voltage of the solar panel is at around the MPP and is taken as 30V.

$$C_1 \geq \frac{I_{O\_max}D_{max}}{2V_{I\_min}f} = \frac{10 \times 1}{2 \times 30 \times 40000} = 4.17\mu\text{F} \quad (3.56)$$

Hence, the chosen capacitor C_1 is 10μF metallized polypropylene film capacitor. This kind of capacitor is bipolar and suitable for high frequency switching. The values of two inductors are chosen as twice the calculated value or $L_1 = L_2 = 0.28\text{mH}$.

3.4.6. Inductor design

Unlike capacitors, which may be bought in the market by the rating of capacitance and voltage range, inductors for switching power applications have to be designed and wound separately.

3.4.6.1. Methodology

An inductor consists of a winding, magnetic core and an air gap. The function of the core is to conduct magnetic field and increase the effect of the magnetic force. A core usually includes an air gap which has a number of advantages. First, it stores most of the energy of an inductor. Second, with the same limit of core saturation, the current flowing in the winding with an air gap can reach higher values than without the air gap. Third, the air gap is less dependent on temperature than the core, so it helps the inductance value be more stable than the core without an air gap.

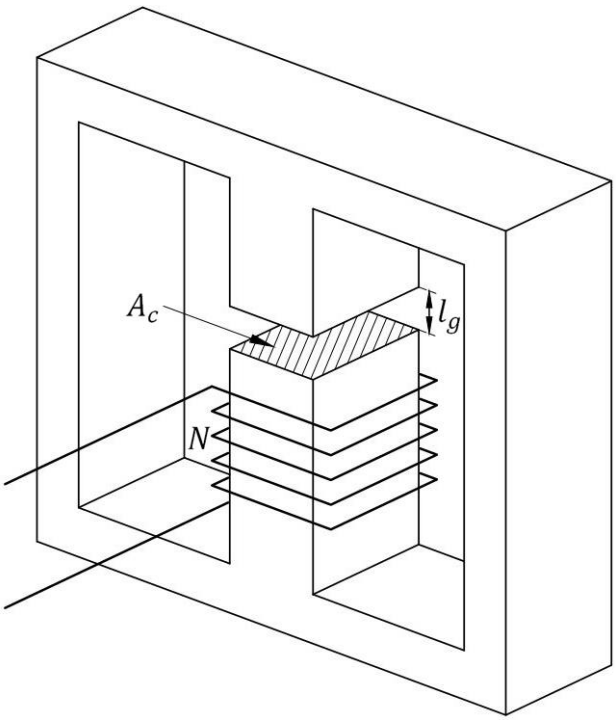

Figure 3.20: Basic E-core inductor

General formulas:

The formula of inductance of an inductor is:

$$L = \frac{N^2}{\mathcal{R}_{eq}} \tag{3.57}$$

Where N is the number of winding turns, $\mathcal{R}_{eq}$ is the equivalent magnetic reluctance of the inductor and it consists of reluctances of core $\mathcal{R}_c$ and the air gap $\mathcal{R}_g$.

$$\mathcal{R}_{eq} = \mathcal{R}_c + \mathcal{R}_g \tag{3.58}$$

$$\mathcal{R}_{eq} = \frac{l_c}{\mu_r \mu_0 A_c} + \frac{l_g}{\mu_0 A_c} = \frac{l_c}{\mu_e \mu_0 A_c} \tag{3.59}$$

with

$$\mu_e = \left(\frac{1}{\mu_r} + \frac{l_g}{l_c}\right)^{-1} \tag{3.60}$$

where l_c is the effective magnetic path length, l_g is the length of the air gap, A_c cross-sectional area of core, μ_0 is the magnetic permeability of free space, μ_r is the relative permeability and μ_e is the effective relative permeability of the core.

From equations (3.57) and (3.59), the inductance value of an inductor is calculated as:

$$L = \frac{N^2 \mu_e \mu_0 A_c}{l_c} \tag{3.61}$$

Litz wire application:

To reduce the effect of Eddy current, Litz wires are used for winding the coil. In this design, 7 insulated strands are used and they are twisted together to make a Litz wire. Litz wire has the advantage of reducing the effect of Eddy current losses since it contains several small diameter strand wires. Moreover, the Litz wire may be easier to bend in comparison to a large solid conductor. For carrying large value of current, several Litz wires are used.

In this section, the formulas are mainly based on the book "Transformers and inductors for power electronics" [54]. In this book, the formulas are applied for single-conductor winding, thus they are different for Litz wires. Therefore, all the formulas will be constructed for this application.

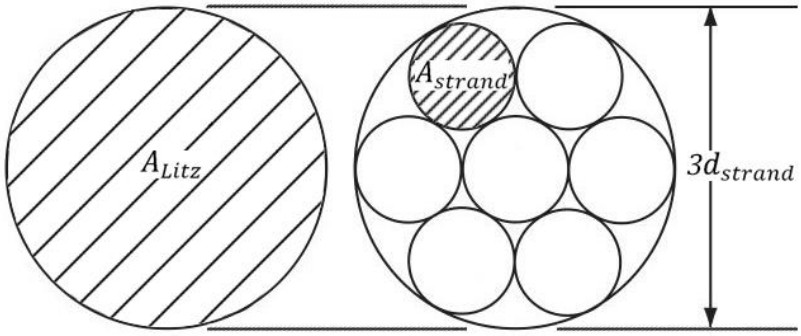

Figure 3.21: Litz wire

Let A_{strand} be the area, d_{strand} be the diameter of each strand. Also for the Litz wire, n_{Litz} is the number of Litz wires and A_{Litz} is the overall area of a Litz wire. The diameter of the Litz wire is approximately three times larger than the strand wire, therefore:

$$A_{Litz} = 9A_{strand} \tag{3.62}$$

Because of winding by hand, the ratio of the winding to the window area of the core is k_u. The relation of the cross-sectional area of the winding to the core window area A_{wd} is shown in the following equation.

$$NA_{Litz}n_{Litz} = 9Nn_{Litz}A_{strand} = k_uA_{wd} \tag{3.63}$$

The Litz wire is made of seven strand wires so that the resistance of the winding R_{wire} is calculated by the resistance of a strand wire divided by seven. In the case of n_{Litz} Litz wires, the winding resistance is reduced because of n_{Litz} connected in parallel.

$$R_{wire} = \frac{\rho l_{wire}}{7n_{Litz}A_{strand}} = \frac{\rho N l_{turn}}{7n_{Litz}A_{strand}} \tag{3.64}$$

where ρ is the resistivity of conductor and l_{turn} is the mean length of a turn of winding wires. The winding wires have resistance so that there is power loss P_{wire} when the current flows. Let I_{L_rms} be the RMS current and k_i be the ratio between RMS and the maximum values of current.

$$P_{wire} = R_{wire}I_{L\_rms}^2 = \frac{\rho N l_{turn}}{7n_{Litz}A_{strand}}k_i^2 I_{L\_max}^2 \tag{3.65}$$

or

$$I_{L\_max} = \frac{1}{k_i}\sqrt{\frac{7n_{Litz}A_{strand}P_{wire}}{\rho N l_{turn}}} \tag{3.66}$$

Also the relationship of inductor current and the flux density is that the largest current flowing to the inductor I_{L_max} causes the flux density to get its maximum value B_{max}.

$$I_{L\_max} = \frac{B_{max}l_c}{\mu_e\mu_0 N} \tag{3.67}$$

Calculating optimum effective permeability:

As seen in (3.65) and (3.67), the higher the current, the higher the power loss and flux density. The dissipation value of the core has to be larger than the loss value of the winding. It is needed for an optimum condition where the maximum current still makes the core under saturation and be lower than the dissipation value. The optimum effective relative permeability μ_{e_opt} occurs when $B_{max} = B_{sat}$ and power loss of the winding wire

equals to the maximum dissipation of the winding P_D or $P_{wire} = P_D$ [54]. From equations (3.67) and (3.66), the value of μ_{e_opt} is calculated as following:

$$\mu_{e\_opt} = \frac{B_{max} k_i l_c}{\mu_0} \sqrt{\frac{9\rho l_{turn}}{7 P_D k_u A_{wd}}} \tag{3.68}$$

Where P_D is calculated by the change in temperature ΔT and the thermal resistance R_θ of the core.

$$P_D = \Delta T / R_\theta \tag{3.69}$$

The value of thermal resistance R_θ can be found in the datasheet of the manufacturer. But in case that the value is not provided, it can be calculated by the volume of the core V_c as:

$$R_\theta = 0.06 / \sqrt{V_c} \tag{3.70}$$

Calculating current density:

The next step is to calculate the current density and it is shown as follow:

$$J_0 = \frac{I_{L\_rms}}{7 n_{Litz} A_{strand}} \tag{3.71}$$

The relationship between winding loss and current density is taken from equation (3.65):

$$P_{wire} = 7\rho N l_{turn} n_{Litz} A_{strand} J_0^2 \tag{3.72}$$

The volume of the wire winding V_w is calculated from equation (3.63) as below:

$$V_w = l_{turn} A_{wd} = 9 l_{turn} N n_{Litz} A_{strand} / k_u \tag{3.73}$$

Combining equations (3.72) and (3.73):

$$P_{wire} = \frac{7}{9} \rho V_w k_u J_0^2 \tag{3.74}$$

Besides the winding loss P_{wire}, there is loss from the core P_{core}. These two power losses are related by the ratio γ. The total loss of the inductor P_{loss} is calculated as:

$$P_{core} = \gamma P_{wire} \tag{3.75}$$

and

$$P_{loss} = P_{core} + P_{wire} = (1 + \gamma) P_{wire} \tag{3.76}$$

Moreover, the total loss P_{loss} depends on the change of temperature ΔT, heat transfer coefficient h_c and the core surface area A_t.

$$P_{loss} = h_c A_t \Delta T \tag{3.77}$$

then

$$(1 + \gamma) P_{wire} = \frac{7}{9} (1 + \gamma) \rho V_w k_u J_0^2 = h_c A_t \Delta T \tag{3.78}$$

Let A_p be the product of core window area A_{wd} and cross-sectional area A_c. The values of V_w and A_t are related with A_p through coefficients k_w and k_a. These coefficients vary for

different types of cores. The typical values of these is found based on extensive studies of several core types and sizes that $k_w = 10$ and $k_a = 40$ [54].

$$A_p = A_c A_{wd} \tag{3.79}$$

$$V_w = k_w A_p^{3/4} \tag{3.80}$$

$$A_t = k_a A_p^{1/2} \tag{3.81}$$

From (3.78) to (3.81), the current density is:

$$J_0 = \frac{1}{\sqrt[8]{A_p}} \sqrt{\frac{9 h_c k_a \Delta T}{7 \rho k_w k_u (1+\gamma)}} = \frac{k_t}{\sqrt[8]{A_p}} \sqrt{\frac{9 \Delta T}{7 k_u (1+\gamma)}} \tag{3.82}$$

with

$$k_t = \sqrt{\frac{h_c k_a}{\rho k_w}} \tag{3.83}$$

Calculating inductor size:

Combining these equations (3.61), (3.67), (3.71) and (3.79), then:

$$L I_{L\_max}^2 = \frac{B_{max} A_p k_u J_0}{k_i} \tag{3.84}$$

After that, substitute J_0 from equation (3.82) to the (3.84), the value of A_p is calculated as:

$$A_p = \left(\frac{k_i L I_{L\_max}^2}{k_t B_{max}} \sqrt{\frac{7(1+\gamma)}{9 k_u \Delta T}} \right)^{\frac{8}{7}} \tag{3.85}$$

Those above equations are used for calculating and choosing the size for the inductor. The following are the steps taken.

Calculating air gap length:

First, the size of the core is determined by the value of A_p from equation (3.85). After that, the length of air gap is chosen by the value of μ_{e_opt} from equation (3.68).

$$l_g \leq \frac{l_c}{\mu_{e\_opt}} \tag{3.86}$$

With the chosen air gap length l_g, the number of turns is calculated as below:

$$N = \sqrt{L / A_L} \tag{3.87}$$

where A_L is the induction factor and depends on the length of the air gap. If the value of the induction factor is not provided, it may be calculated as following:

$$A_L = \frac{\mu_0 A_c}{\left(\frac{l_c}{\mu_r} + \frac{l_g}{k_g} \right)} \tag{3.88}$$

With k_g is the air gap correction coefficient and is the practical correction for l_g. The table below shows the values of k_g [55].

l_g (mm)	0.1	0.2	0.5	1.0	2.0	3.0	4.0
k_g	1.1	1.2	1.3	1.4	1.5	1.65	1.8

Table 3.6: Values of the air gap correction

Calculating Litz wire:

The next step is choosing the size of the strand wires. The diameter of the wire should be close to half of the skin depth δ.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} \tag{3.89}$$

and

$$d_{strand} \approx \frac{\delta}{2} \tag{3.90}$$

With the chosen wire size, the number of Litz wire needed to use for carrying enough current is calculated through the current density J_0 from equation (3.71):

$$n_{Litz} = \frac{k_i I_{L\_max}}{7 J_0 A_{strand}} \tag{3.91}$$

Calculating the power losses:

The following step is determining the wire and core losses. The power loss of the winding is calculated:

$$P_{wire} = R_{wire} I_{L\_rms}^2 = \frac{\rho N l_{turn}}{7 n_{Litz} A_{strand}} I_{L\_rms}^2 \tag{3.92}$$

with

$$\rho = \rho_0 [1 + \alpha_0 (T_{max} - 20)] \tag{3.93}$$

The core loss is proportional to the volume V_c of the core, the frequency f of current and the change of flux density ΔB.

$$P_{core} = V_c k_{core} f^{\alpha} \left(\frac{\Delta B}{2}\right)^{\beta} \tag{3.94}$$

Where α, β and k_{core} are coefficients of material making the core.

3.4.6.2. Calculation for the inductor

The material for the core of this application is ferrite N87, which is suitable for high frequency. With the initial conditions in the table below, the size of the core will be

determined. The maximum operating temperature of both the core and winding wire is 155°C, so that the maximum temperature T_{max} for calculation is taken half of it or 70°C.

L = 0.28mH	k_u = 0.5	B_{max} = 0.2T
I_{L_max} = 8.5A	γ = 0	k_{core} = 16.9
k_i = 1	ΔT = 40°C	α = 1.25
f = 40kHz	T_{max} = 70°C	β = 2.35

Table 3.7: Initial values for calculating inductor

From equation (3.85), A_p is calculated as:

$$A_p = \left(\frac{(0.28 \times 10^{-3}) \times 8.5^2}{(48.2 \times 10^3) \times 0.2} \sqrt{\frac{7}{9 \times 0.5 \times 40}} \right)^{\frac{8}{7}} = 5.07\text{cm}^4 \quad (3.95)$$

Choose the core ETD49 which has the A_{p_ETD49} = 5.8cm^4.

A_{wd} = 2.75cm^2	l_{turn} = 8.7cm	V_c = 24.1cm^3
A_c = 2.11cm^2	μ_r = 1630	l_c = 11.4cm

Table 3.8: Specifications of ferrite core ETD49 [56]

Thermal resistance can be taken from equation (3.70) as:

$$R_\theta = 0.06/\sqrt{24.1 \times 10^{-6}} = 12.2\text{°C/W} \quad (3.96)$$

Therefore, the maximum dissipation power of the core is:

$$P_D = 40/12.2 = 3.27\text{W} \quad (3.97)$$

From equation (3.93), the resistivity of conductor at the temperature of T_{max} is:

$$\rho = (1.72 \times 10^{-8})[1 + 0.004(70 - 20)] = (2.06 \times 10^{-8})\Omega\text{m} \quad (3.98)$$

Then the optimum effective relative permeability is taken from equation (3.68) as:

$$\mu_{e\_opt} = \frac{0.2 \times 0.114}{4\pi \times 10^{-7}} \sqrt{\frac{9(2.06 \times 10^{-8}) \times 0.087}{7 \times 3.27 \times 0.5 \times (2.75 \times 10^{-4})}} = 41.13 \quad (3.99)$$

The condition for choosing the gap length is then taken from equation (3.86):

$$l_g \leq \frac{0.114}{41.13} = 2.77\text{mm} \quad (3.100)$$

Choose the length of air gap l_g=2.5mm, then to calculate the number turn, the value of A_L needs to be determined. However, the datasheet of the core does not show the value for a

gap of 2.5mm. Therefore, it is determined from equation (3.88). From Table 3.6, the value of k_g is calculated as 1.575, then:

$$A_L = \frac{(4\pi \times 10^{-7})(2.11 \times 10^{-4})}{\left(\frac{0.114}{1630} + \frac{(2.5 \times 10^{-3})}{1.575}\right)} = 1.6\text{nH} \tag{3.101}$$

The number of turn is calculated from equation (3.87):

$$N = \sqrt{(0.28 \times 10^{-3})/(1.6 \times 10^{-9})} = 41.8 \tag{3.102}$$

Choose $N = 42$ turns. The next step is to determine the size of winding wire. First, the skin depth is calculated:

$$\delta = \sqrt{\frac{(2.06 \times 10^{-8})}{40000\pi(4\pi \times 10^{-7})}} = 0.362\text{mm} \tag{3.103}$$

From the condition in (3.90), choose $d_{strand} = 0.4$mm or $A_{strand} = 0.136\text{mm}^2$. The current density is calculated as below from equation (3.82):

$$J_0 = \frac{(48.2 \times 10^3)}{\sqrt[8]{(5.8 \times 10^{-8})}} \sqrt{\frac{9 \times 40}{7 \times 0.5}} = 3.924\text{A/mm}^2 \tag{3.104}$$

Use the value of J_0 to calculate the number Litz wires n_{Litz} from equation (3.91):

$$n_{Litz} = \frac{8.5}{7(3.924 \times 10^6)(0.136 \times 10^{-6})} = 2.28 \tag{3.105}$$

Choose $n_{Litz} = 3$. From equation (3.63), the window utilization factor is calculated as:

$$k_{u\_after} = \frac{9A_{strand}n_{Litz}N}{A_{wd}} = \frac{9 \times (0.136 \times 10^{-6}) \times 3 \times 42}{(2.75 \times 10^{-4})} = 0.56 \tag{3.106}$$

The window utilization factor is about 0.6 which is hard for winding manually. Therefore, the designer should make the winding very carefully. Parameters needed for making an inductor are now all calculated. The laboratory inductors are shown in Figure 3.22.

The next step is to calculate the power loss of the inductor. From equation (3.65), the wire loss is then calculated as:

$$P_{wire} = \frac{(2.06 \times 10^{-8}) \times 42 \times 0.087 \times 8.5^2}{7 \times 3 \times (0.136 \times 10^{-6})} = 1.91\text{W} \tag{3.107}$$

Core loss is determined with the value $\Delta B = 0.2$T which is chosen to be equal the maximum flux density of the core. Therefore from equation (3.94), P_{core} is calculated as:

$$P_{core} = (24.1 \times 10^{-6}) \times 16.9 \times 40000^{1.25} \left(\frac{0.2}{2}\right)^{2.35} = 1.03\text{W} \tag{3.108}$$

Then the total loss of the core and the winding is:

$$P_{loss} = 1.03 + 1.91 = 2.94\text{W} \tag{3.109}$$

The maximum total loss of one inductor is calculated of 2.94W. The loss in practical operation may be less than this value because the loss is calculated in the most extreme condition.

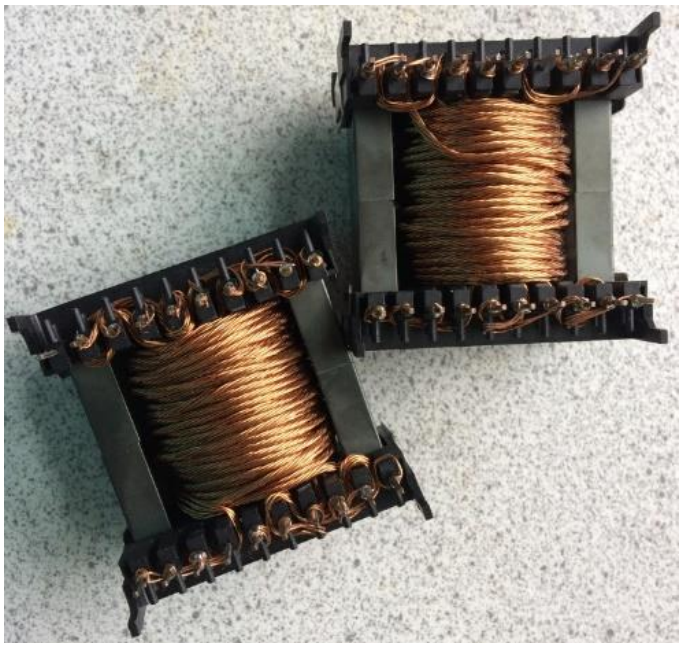

Figure 3.22: Implemented inductors

In Figure 3.23, the inductance of the implemented inductor is measured by an LCR meter and the result is 0.280mH which is the exact value needed.

In comparison to the method using single wire, the core size is calculated as below [54].

$$A_{p\_single} = \left(\frac{k_i L I_{L\_max}^2}{k_t B_{max}} \sqrt{\frac{1+\gamma}{k_u \Delta T}} \right)^{\frac{8}{7}} \tag{3.110}$$

The difference between the method of using a single conductor and using Litz wires is:

$$\frac{A_{p\_Litz}}{A_{p\_single}} = \left(\sqrt{7/9}\right)^{\frac{8}{7}} = 0.866 \tag{3.111}$$

From equation above, the core size using single conductor is 15% larger than the core using Litz wires.

Figure 3.23: Measurement of the inductor

3.5. Programming

A Tiva C Series TM4C123G LaunchPad Evaluation Board from Texas Instruments is used for control system. The board includes In-circuit Debug Interface (ICDI) that allows easy programming and debugging of the microcontroller. It also includes two PWM modules and two 12-bit Analog-to-Digital Converter (ADC) modules, which are convenient to get measured quantities and control all power converters.

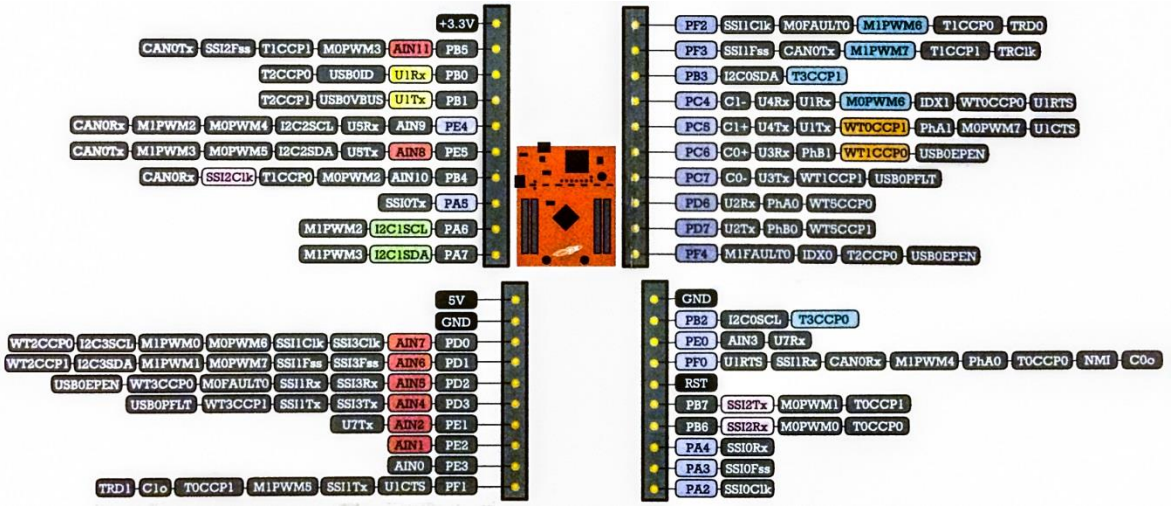

Figure 3.24: Pin diagram of TM4C123G LaunchPad Evaluation Board [57]

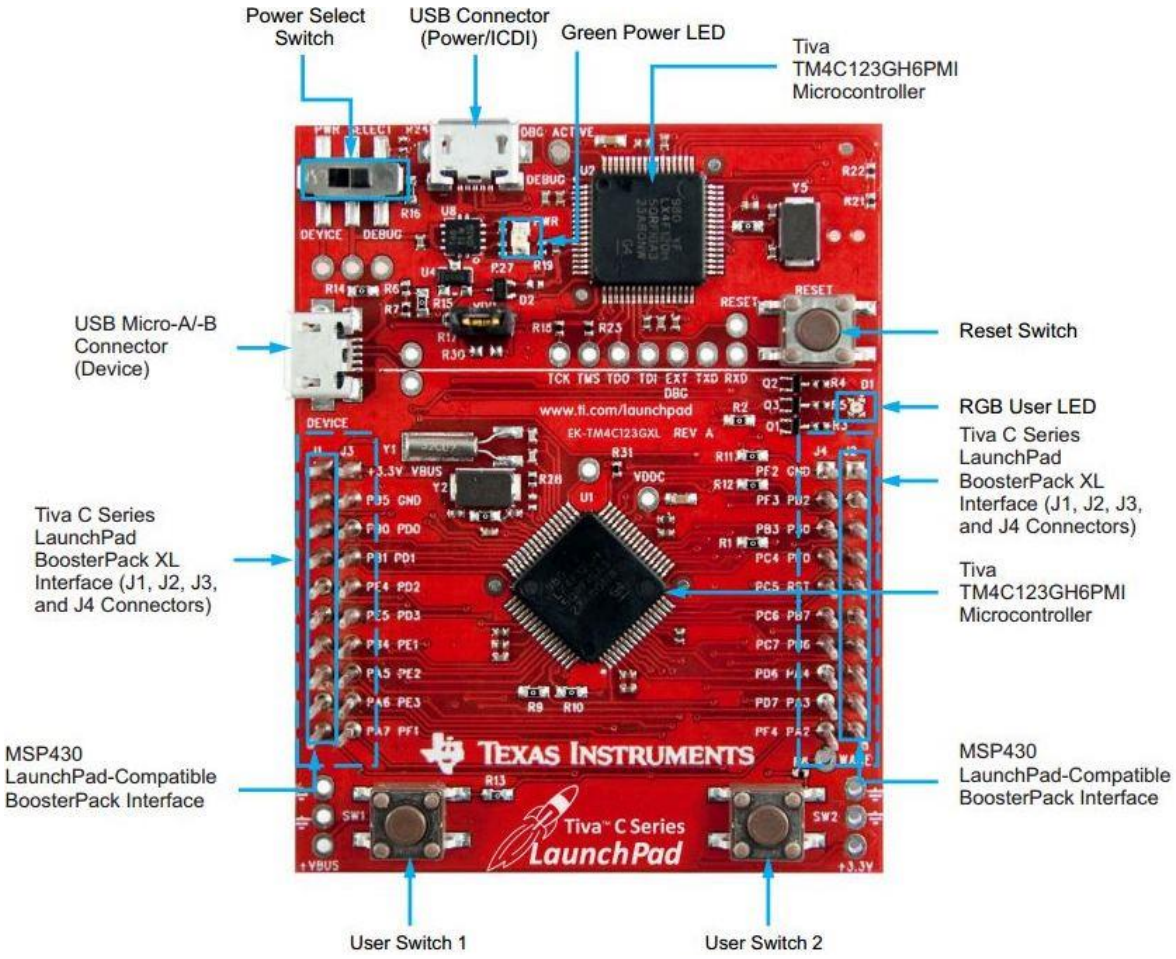

Figure 3.25: Tiva C Series TM4C123G LaunchPad Evaluation Board [58]

The environment for programming is the CCS software, which the values of variables in the microcontroller memory can be exported to a laptop.

Timer0 is set at 50Hz and is used for updating duty cycle and measuring values of voltage and current.

To measure current and voltage values of PV, the ratio of real voltage and sensor is measured in advance. As mentioned in section 3.4.4, the ratio of voltage is measured of 14.1, therefore the PV voltage is calculated as the equation below.

$$V_{PV} = (V_{ADC} \times 3.3/4095) \times 14.1 \quad (3.112)$$

For the current, the formula is based on the datasheet of the current transducer.

$$I_{PV} = ((V_{ADC} \times 3.3/4095) \times 1.03 - 2.524) \times 9.6 \quad (3.113)$$

Pins PD0 and PD1 are taken to be the input pins to measure PV current and voltage respectively.

The module ADC0 is used. The data capture and sampling control are handled by the sample sequencers. The sequencer SS0 is chosen because it contains 8 samples to be stored. By using the hardware averaging circuit, 64 samples are accumulated and averaged to form each of the 8 single data entries in the sequencer. This means that the actual number of samples stored in the sequencer SS0 is 512. The ripple and noise in the PV current input are more than in the PV voltage input. Therefore, among the 8 entries of SS0, 2 entries are used for measuring the PV voltage value and the rest of 6 entries are taken for the current value. This means 128 samples in total are for voltage value and 384 samples are taken average for the current value in every 20ms. This results in lower noise and higher precision. The detail coding can be seen in the Appendix.

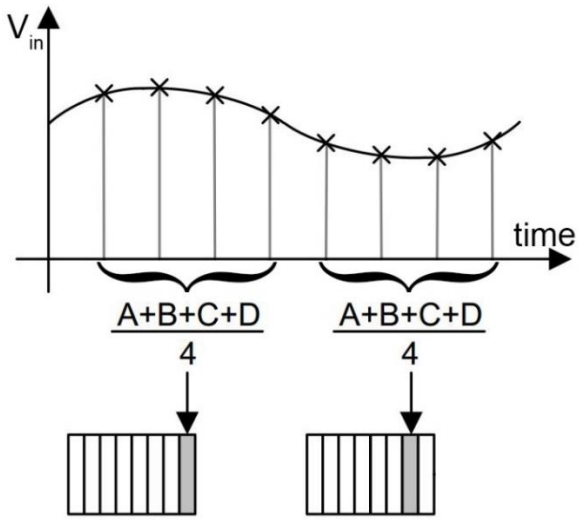

Figure 3.26: Example of ADC 4-sample averaging of sequencer SS0

3.6. Experimental results

In this section, the operation of the DC/DC converter and the effectiveness of MPPT algorithms will be tested. The SEPIC circuit needs to be tested first to make sure it will operate as expected. The experimental results will be compared to the simulation. The MPPT is then verified, its efficiency and dynamic response are measured.

3.6.1. SEPIC circuit

The experiment SEPIC circuit was designed as in Figure 3.27 below. The input and output capacitors include two types of tantalum and electrolytic capacitors as mention in section 3.4.1. The voltage rating of the tantalum capacitors is 50V [59] which is higher than the

input and output of the circuit so that they can be placed in parallel to the large electrolytic capacitors for reducing noise.

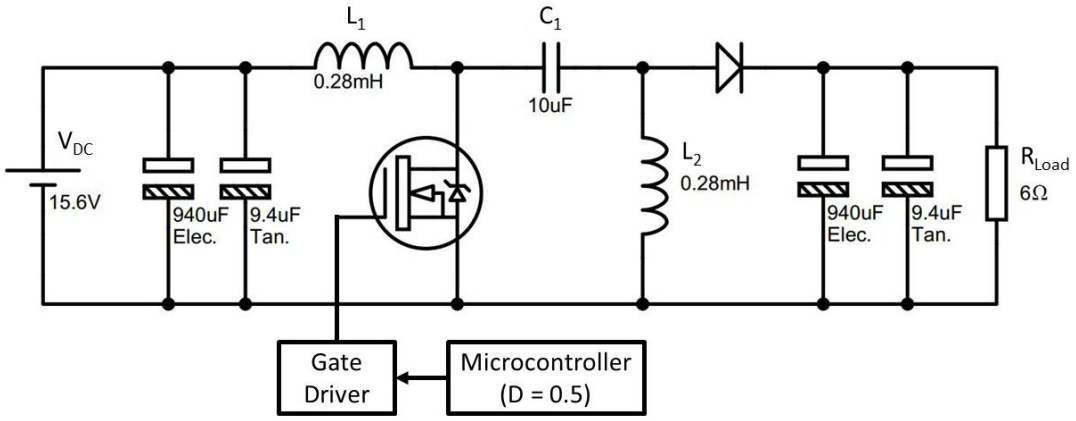

Figure 3.27: Experimental SEPIC circuit for performance testing

The duty cycle D is set to the value of 0.5, so that from equation (3.23), the input and output voltage theoretically should be equal to each other. The DC input voltage of SEPIC is set to be 15.6V and the output is connected to a 6Ω resistor. The MATLAB simulation of the SEPIC whose component values are the same as in Figure 3.27 is also conducted and put to the graph with the experimental results for comparison.

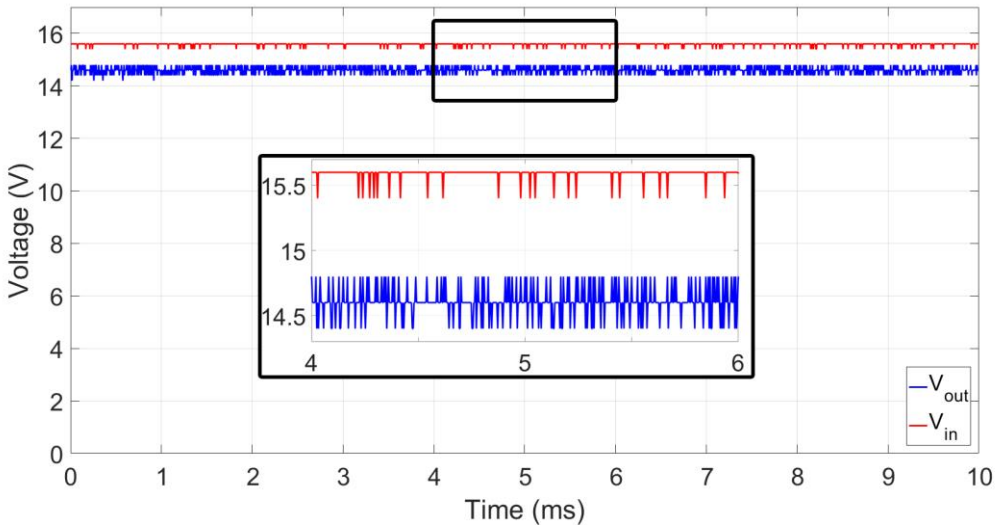

Figure 3.28: Experiment result of SEPIC input and output voltages

In Figure 3.28, the measured output voltage is 14.6V, which is 1V less than the input level because of the voltage drop of the output diode. In comparison to the input voltage, the output voltage does not consist of large ripples. The following figures show the voltage waveforms of components in the circuit.

In Figure 3.29, the C_1 voltage oscillated around the input voltage of 15.6V. From equation (3.34), the voltage ripple of the capacitor is calculated as:

$$\Delta v_{C_1} = \frac{DI_O}{C_1 f} = \frac{DV_O}{C_1 f R} = \frac{0.5 \times 14.6}{(10 \times 10^{-6}) \times 40000 \times 6} = 3\text{V} \qquad (3.114)$$

As seen in Figure 3.29, the voltage variation of the capacitor C_1 is around 3V which is similar to the calculated one. Besides, the capacitor voltage consists of high frequency harmonics but they are not too high to affect the output results of the converter.

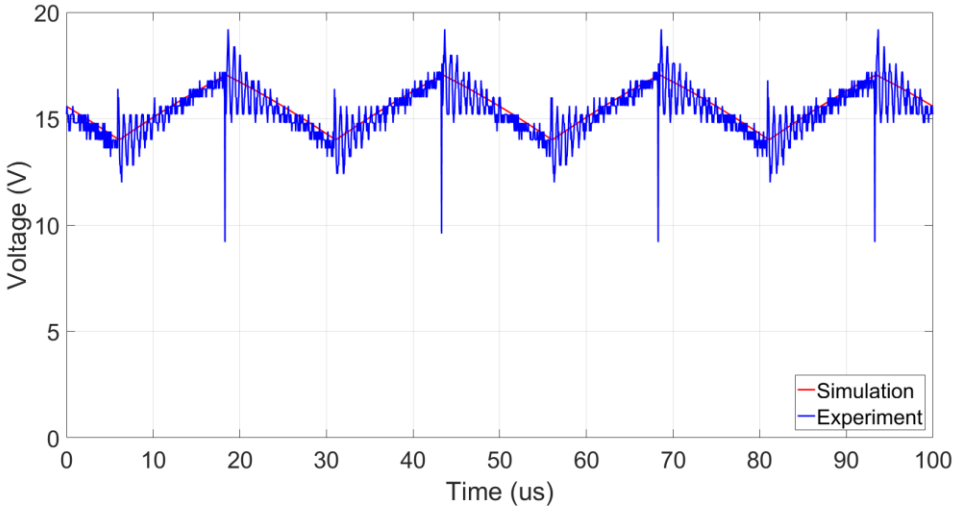

Figure 3.29: Experiment and simulation results of SEPIC C_1 voltage

In Figure 3.30, the voltage of L_1 is in positive side when the switch is closed and in negative side when the switched is opened. When V_{L_1} is positive, its value is 15.6V which is equal the input voltage. At the negative side, the voltage ripples is about 3V which is similar to the ripple in the capacitor C_1.

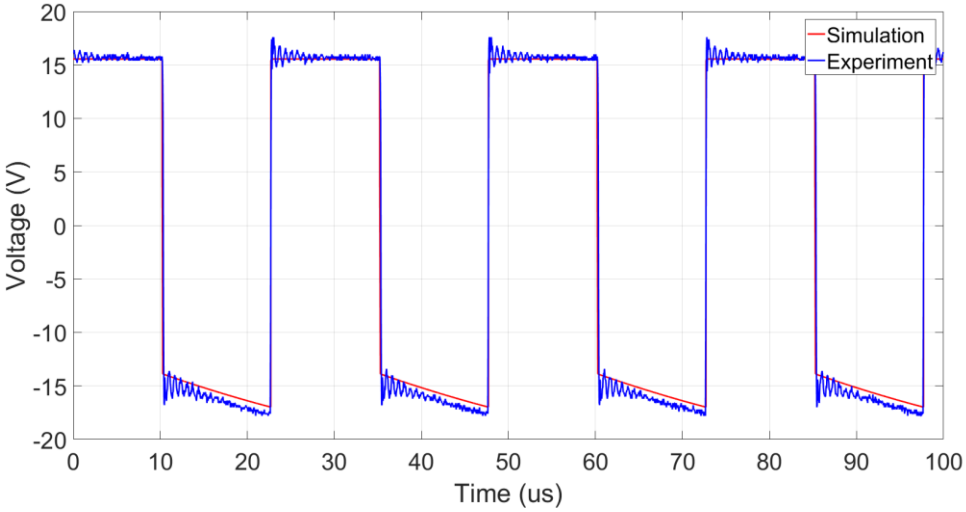

Figure 3.30: Experiment and simulation results of SEPIC L_1 voltage

Similar to the L_1, in Figure 3.31, the voltage of the inductor L_2 is positive when the switched is closed and negative when the switch is opened. The average value in the positive side equal to 15.6V and the voltage variation is also around 3V. In both waveforms of the two inductors, the high frequency contents still exist but their amplitudes are small and are filtered by the capacitor at the output.

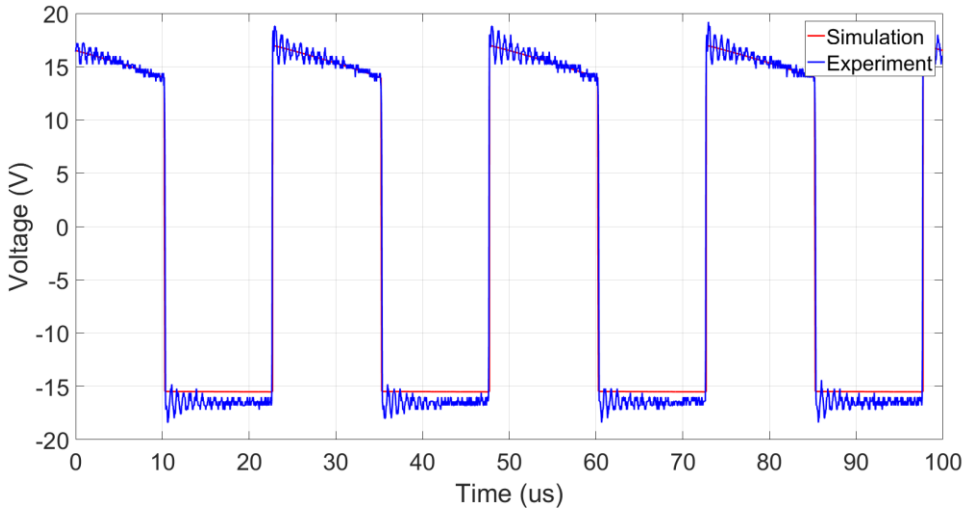

Figure 3.31: Experiment and simulation results of SEPIC L_2 voltage

As seen in Figure 3.32, the switch voltage is nearly zero when it is closed. When the switch is opened, the measured average value is 31.1V which as twice as the input voltage. As the theory shown in Figure 3.2, the rise of the voltage when the switch is opened equals to the sum of ripples in the capacitor C_1 and the output voltage. Since the output voltage has insignificant ripple so that the voltage rise of the switch when it is opened is similar to the ripple of C_1 or 3V.

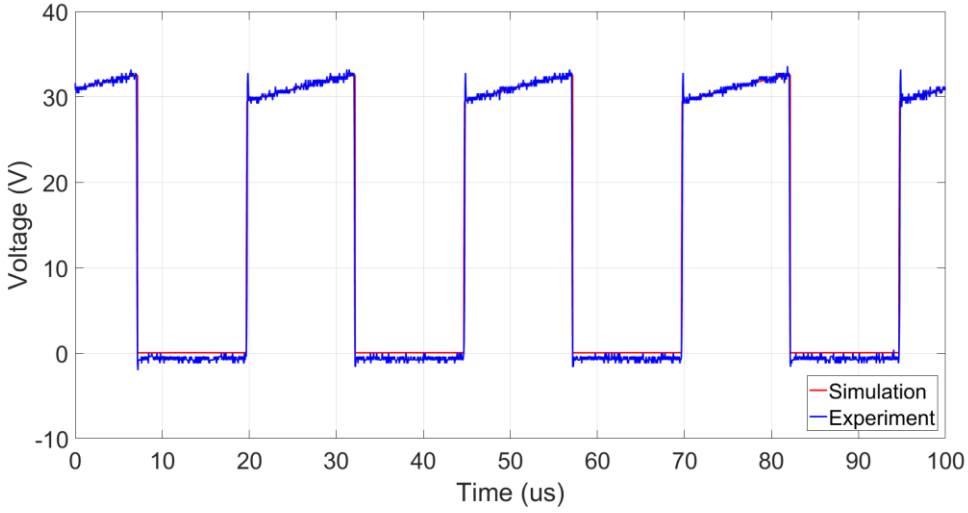

Figure 3.32: Experiment and simulation results of SEPIC switch voltage

In Figure 3.33, the diode voltage is negative when the switch is closed and its average value is about -31V. When the switch is opened, the diode conducts and the voltage drop on it is measured about 1V.

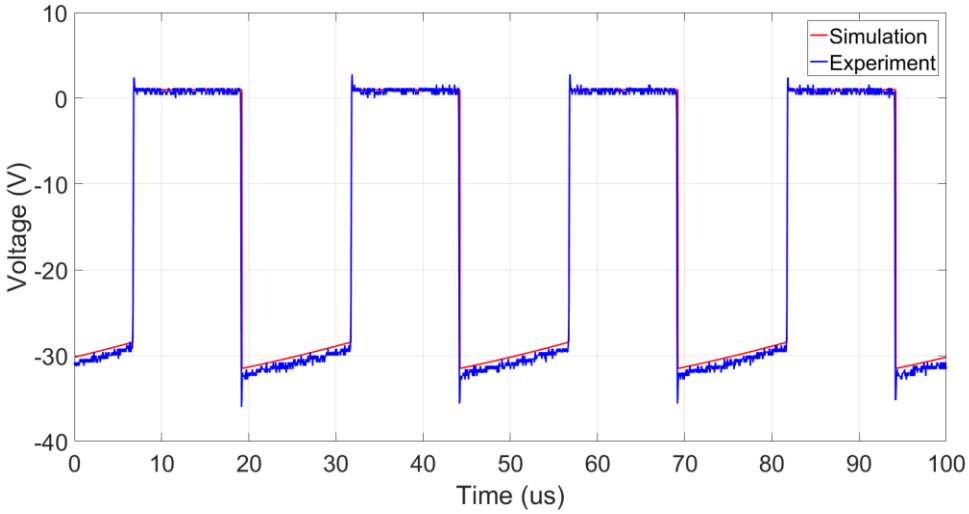

Figure 3.33: Experiment and simulation results of SEPIC diode voltage

In conclusion, the results from the experiment are similar to the theory depicted in Figure 3.2. Therefore, the design of SEPIC satisfies the continuous mode and qualifies for the next step, which is the testing the effectiveness of MPPT methods.

3.6.2. MPPT test

The test for MPPT was carried out in the Zero2020 electrical control room of Cork Institute of Technology.

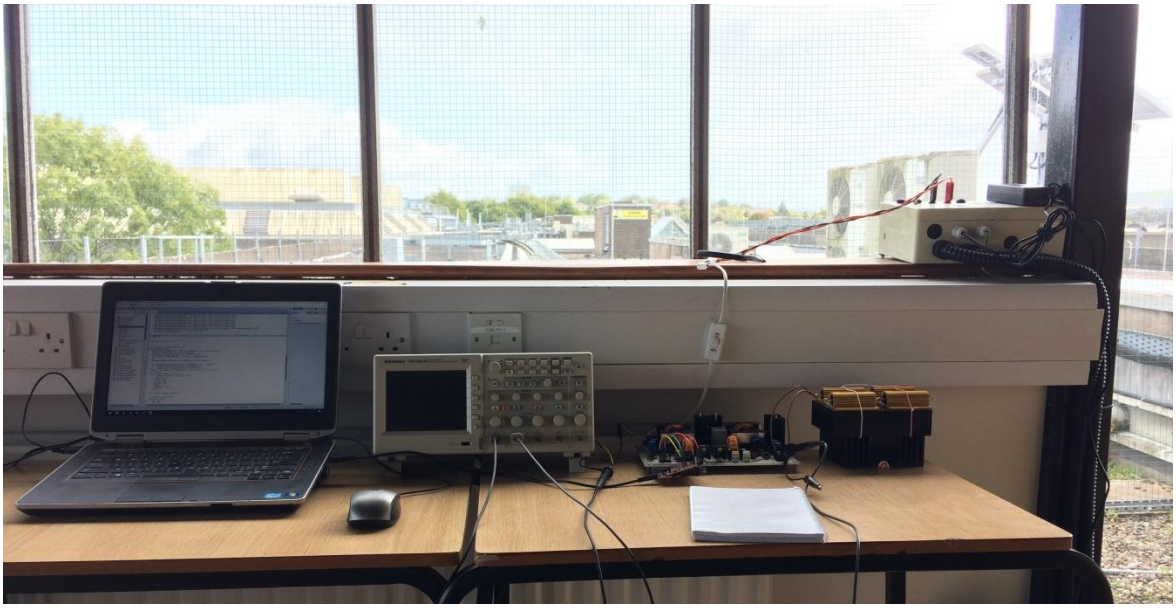

Figure 3.34: MPPT testing set-up

DC wires from the tested solar module are routed to the room for the experiment. The voltage and current values of the panel are recorded in the microcontroller memory and then are read by the CCS software installed in a laptop.

The circuit is connected as Figure 3.35 below. The component values of the SEPIC circuit are the same as in Figure 3.27. The voltage and current sensors are connected to get data for the microcontroller. The microcontroller makes decisions using the MPPT algorithm and outputs the PWM signal to the MOSFET gate driver for controlling the circuit.

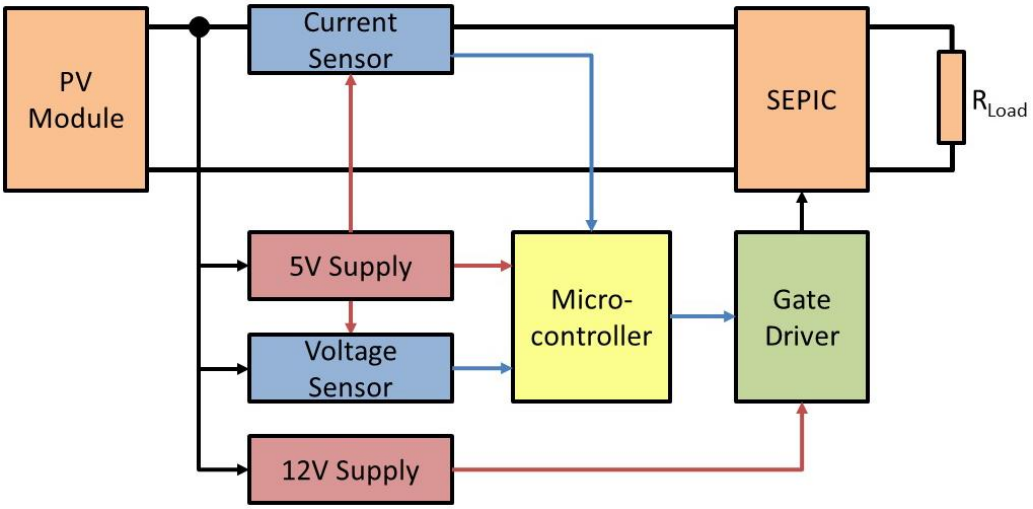

Figure 3.35: Block connection of the MPPT testing

The output of the SEPIC is connected to four 1.5Ω–100W resistors connected in series giving an equivalent 6Ω–400W output resistor. The maximum output power of PV panel is about 280W and voltage of 35V, therefore a 6Ω resistor is suitable.

Figure 3.36: Output resistors for MPPT testing

Controlling and switching frequencies for the circuit are the same as the Table 3.3. Other controlling values for the experiment are: ε_P = 1 W, ε_D = 0.001. Current and voltage values are obtained by the ADC of the microcontroller every 0.02s.

Two criteria for an MPPT method are the efficiency of the algorithm and the response time to the change in irradiance.

3.6.2.1. Efficiency test

In the test, the pyranometer SP Lite2 [60] is used for measuring the incident irradiance. It is placed and tilted with the same angle as the tested solar module.

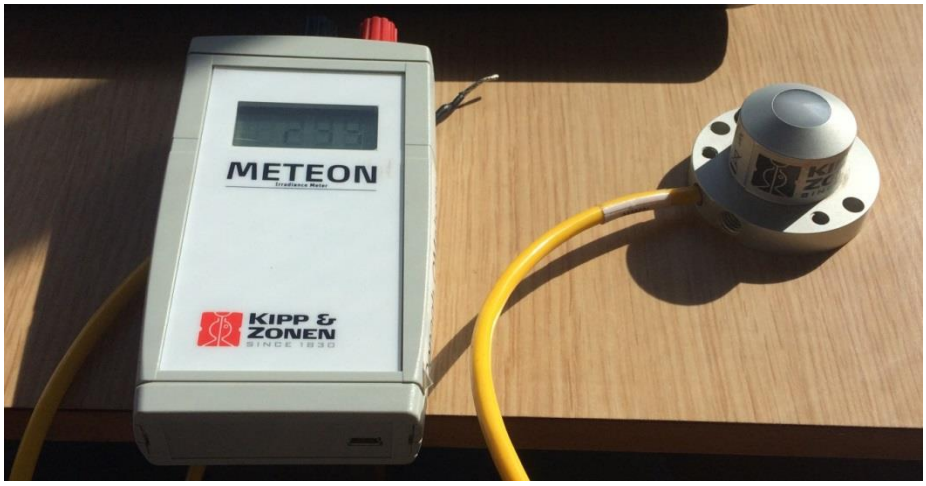

Figure 3.37: Pyranometer SP Lite2

The output power of the solar module depends not only the irradiance but also the temperature of the panel.

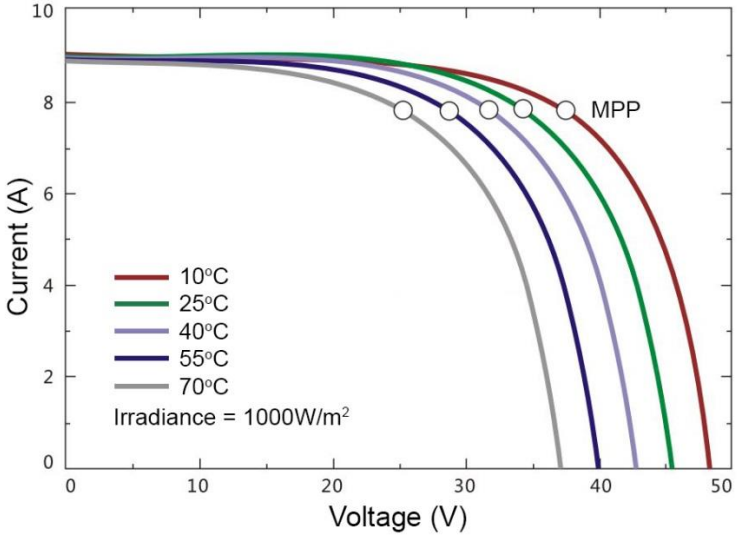

Figure 3.38: PV Current-Voltage curve of different temperatures [61]

In Figure 3.38, the MPP of the PV module decrease when the cell temperature increases. To determine the efficiency of the algorithm, the power at MPP taken from the solar panel is theoretically calculated as below. The parameters are taken from Table 3.5.

$$P_{MPP} = P_{\max\_STC}\frac{G}{G_{STC}}\left(1+\eta_P(T-T_{STC})\right) \quad (3.115)$$

or

$$P_{MPP} = 280\frac{G}{1000}\left(1-0.00459(T-25)\right) \quad (3.116)$$

Where G is the irradiance value read from the pyranometer. The temperature T is taken from the temperature sensor installed under a solar module, which is near the tested one as in Figure 3.39 below.

Figure 3.39: Temperature sensor location for the experiment

The efficiency of the MPPT algorithm is then calculated by the formula below.

$$\eta_{MPPT} = \frac{P_{measured}}{P_{MPP}} \quad (3.117)$$

There are errors in measurement from the solar module power tolerance, temperature and irradiance sensors. In addition, because there is just one solar module for the experiments, each test is conducted in a specific condition and the experiments for different MPPT methods are carried out in different time, irradiation and temperature. Thus, the results of the experimental efficiency are relative and used for comparison among different MPPT algorithms.

In this experiment, the algorithms are tested to investigate the most efficient method and validate the simulation and theory. In Figure 3.40, the results of modified P&O are presented. As the previous discussion, the voltage fluctuation leads to ripples in the power

result. In the experiment, the algorithm operates as the traditional P&O because the |ΔP| is larger than the value ε_{PO} as shown in the simulation section. The efficiency of this method is 96.76%.

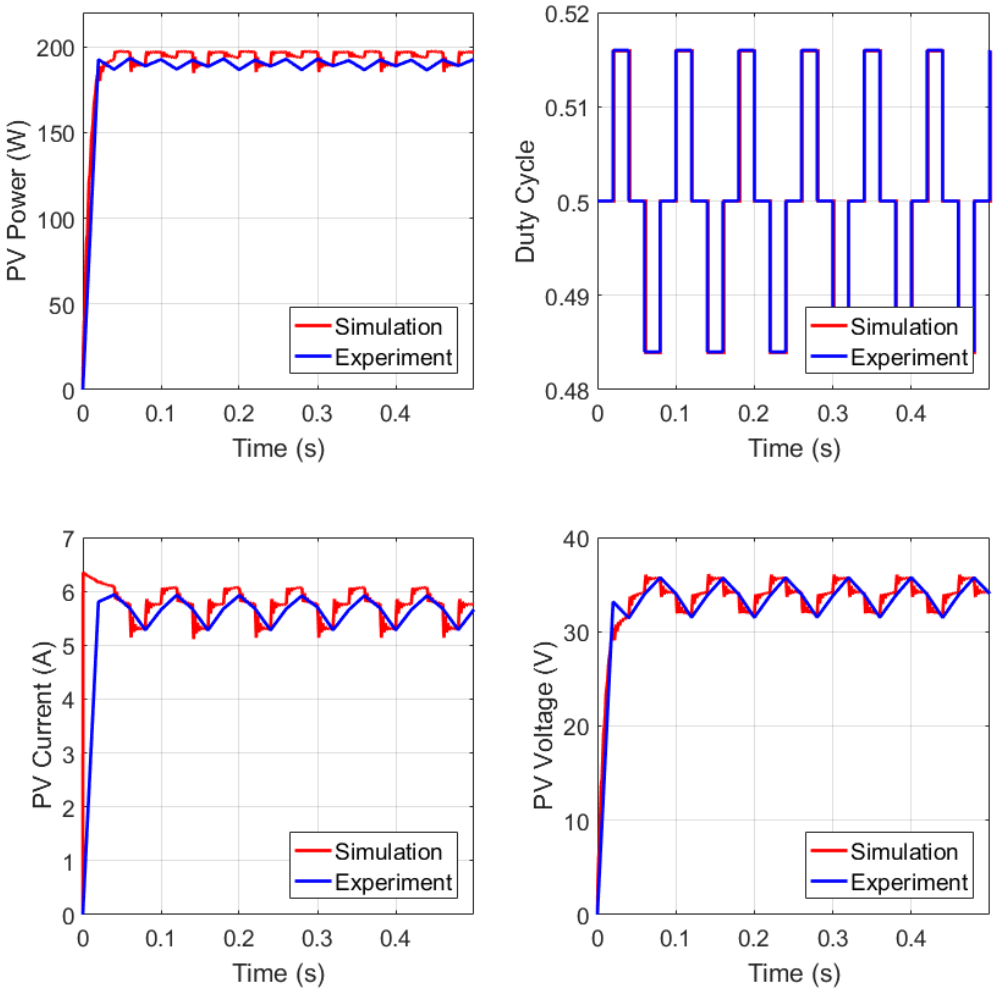

Figure 3.40: Experiment and simulation results of modified P&O

The experimental results of BS-P&O algorithm are shown in Figure 3.41. The efficiency of this method is measured at 99.23%. It is 2.5% higher than the tested modified P&O. Moreover, the BS-P&O method makes the PV voltage and current values not vary at the MPP. In addition, it can be seen that the time for the algorithm to reach the MPP is fast and less than 0.2s.

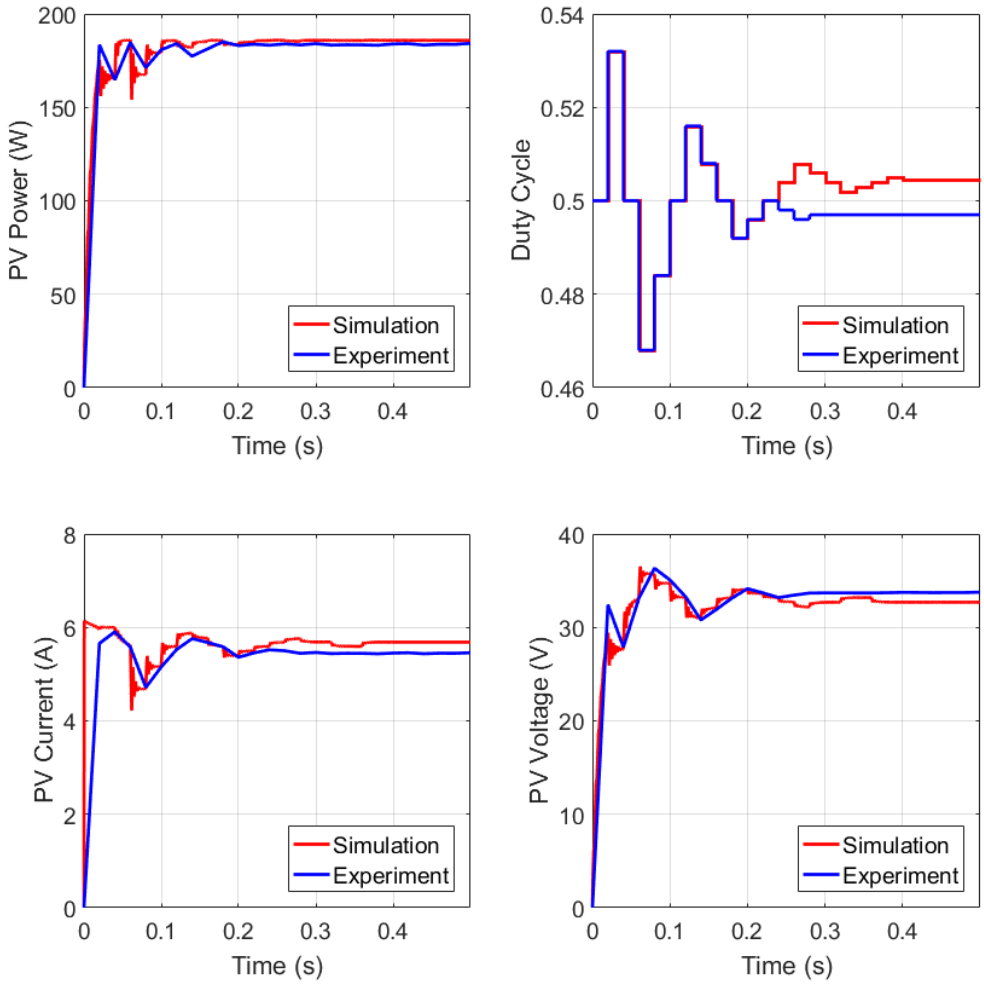

Figure 3.41: Experiment and simulation results of BS-P&O

The table below is the summary for the experimental results of the efficiency of the two methods.

MPPT method	Modified P&O	BS-P&O
Step size ΔD_0	0.016	0.016
Irradiation G	758W/m^2	732W/m^2
Temperature T	40.9°C	46.3°C
P_{MPP}	196.75W	184.92W
$P_{measured}$ (average steady state)	190.38W	183.50W
Efficiency η_{MPPT}	96.76%	99.23%
Ripple (steady state)	5W	0.3W

Table 3.9: Experimental efficiency comparison of MPPT methods

3.6.2.2. Response test

In this test, the solar module is initially set to reach the MPP, then it is partially covered for about one second and then uncovered for the rest of time. This experiment measures the response time of the algorithm under sudden changes in the environment.

Figure 3.42 shows the response test of the modified P&O method. Similar to the simulation in Figure 3.12, the system fluctuated around MPP at the irradiation when tested. The system responses to the shaded condition in less than 0.1s and stops fluctuating in the time of shading.

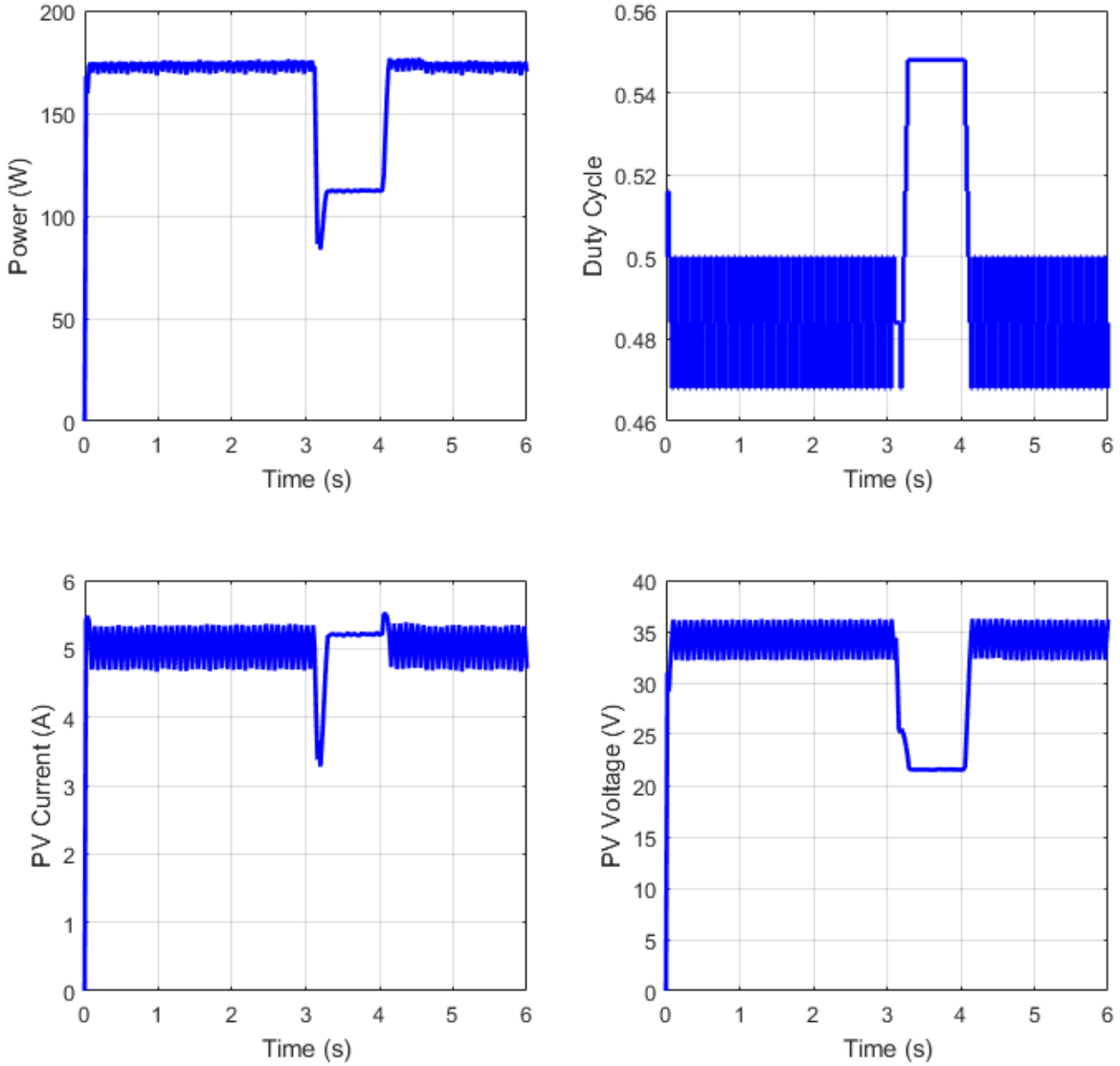

Figure 3.42: Experiment results of modified P&O response

As it can be seen in Figure 3.43 that panel power drops quickly due to the change in irradiance, and then it soon moves to the new point. The change in duty cycle and the

voltage are large in the transition and become smaller to get closer to the MPP. The response time of BS-P&O algorithm is less than 0.2s, which is similar to the simulation and proves its effectiveness.

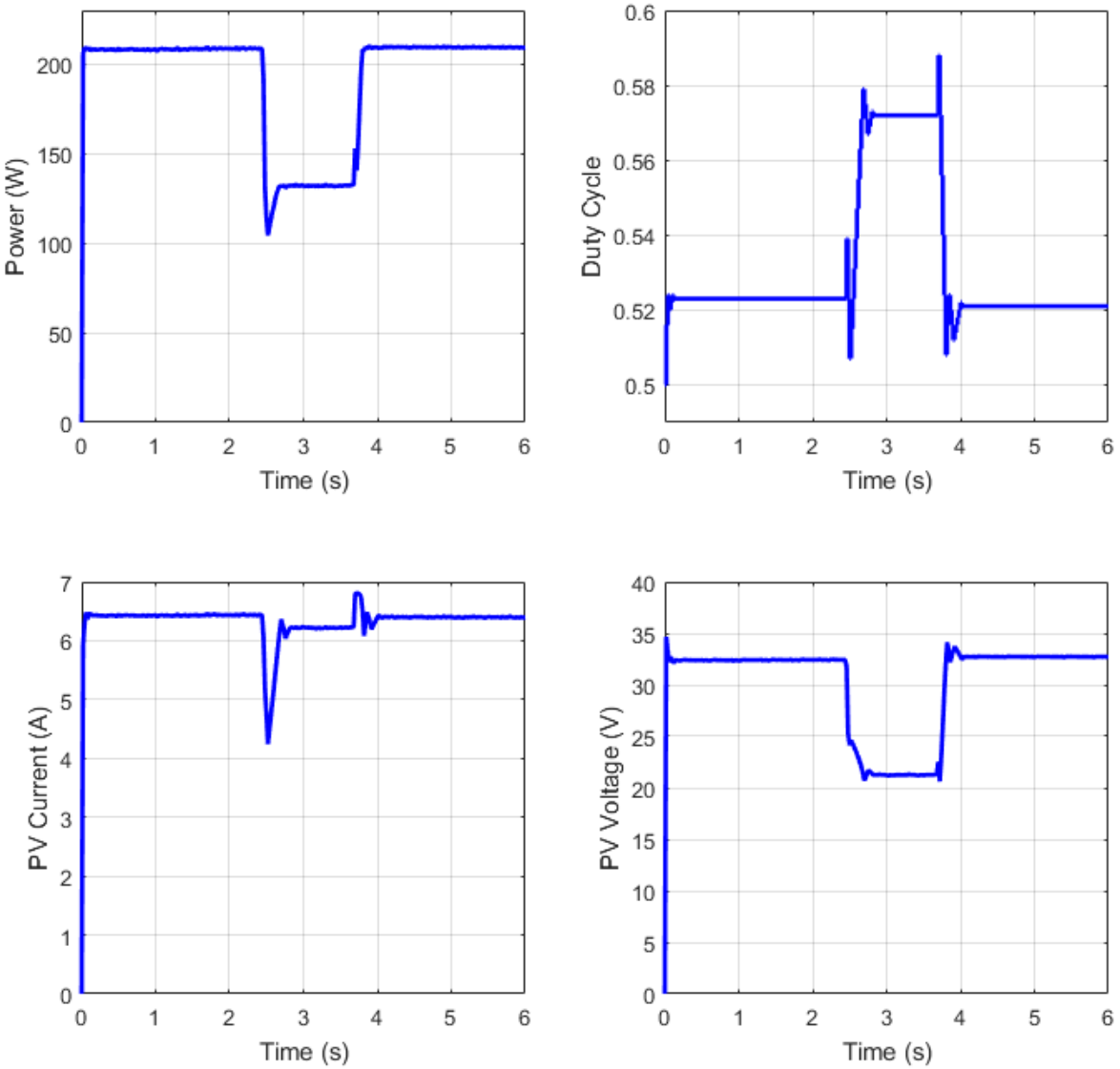

Figure 3.43: Experiment results of BS-P&O response

In conclusion, the BS-P&O has been proven the effectiveness and quick response for the MPPT task from the simulation to the experiment. This method can reach MPP of solar modules exactly and quickly and is better than the traditional P&O and modified P&O methods.

In this chapter, the SEPIC was selected and it was proven to meet criteria of the research. The SEPIC was also used for verifying the novel BS-P&O method which had a better performance than the modified P&O. The next chapter is the DC/AC circuit design which includes the power topology and grid measurement method.

CHAPTER 4. DC/AC CIRCUIT DESIGN

In this chapter, the design and implementation of the DC/AC converter is presented. The topology of the converter is tested in simulation and experiment. The design of grid measurement methods is also mentioned and the sensor circuits are tested with the grid.

4.1. Theory

In this section, the topology of the DC/AC converter is introduced and its operating is described. In addition, an approach of controlling the inverter to export the active and reactive powers to the grid is presented.

4.1.1. Power topology

The output voltage of the DC/DC converter is low in comparison to grid level. Therefore, using a transformer to boost voltage is needed in the DC/AC converter. It is known that higher the frequency of the signal, the smaller the size of transformer needed. To keep the size of transformer small, its input should be at high frequency. The topology for the inverter will be discussed to meet all the above criteria.

Figure 4.1 is the typical 3-level sinusoidal PWM (SPWM) waveform of a H-bridge output. The PWM waveform is created by comparing a high frequency triangle waveform to a reference sine waveform. The frequency of SPWM is also the frequency of the triangle waveform. This SPWM waveform is then filtered to output the pure sinusoidal wave. The amplitude of the filtered sine wave is depended on the ratio of the reference sine waveform to the triangle one. The frequency in Figure 4.1 is 4kHz which is used for just the illustration purpose. With higher frequencies, the PWM waveform cannot be seen. The frequency used in the application is 40kHz.

In Figure 4.2, the Fast Fourier Transform (FFT) is applied for the waveform which is similar the one in Figure 4.1 but at the frequency of 40kHz. The main component with the highest amplitude is at 50Hz with the amplitude of 0.5923, while the carriers of 40050Hz and 39950Hz have the levels of 0.3619 and 0.3788 respectively. For this reason, the waveform in Figure 4.1 cannot be used to pass through a high frequency transformer. Another approach is carried out to avoid the low frequency spectrums.

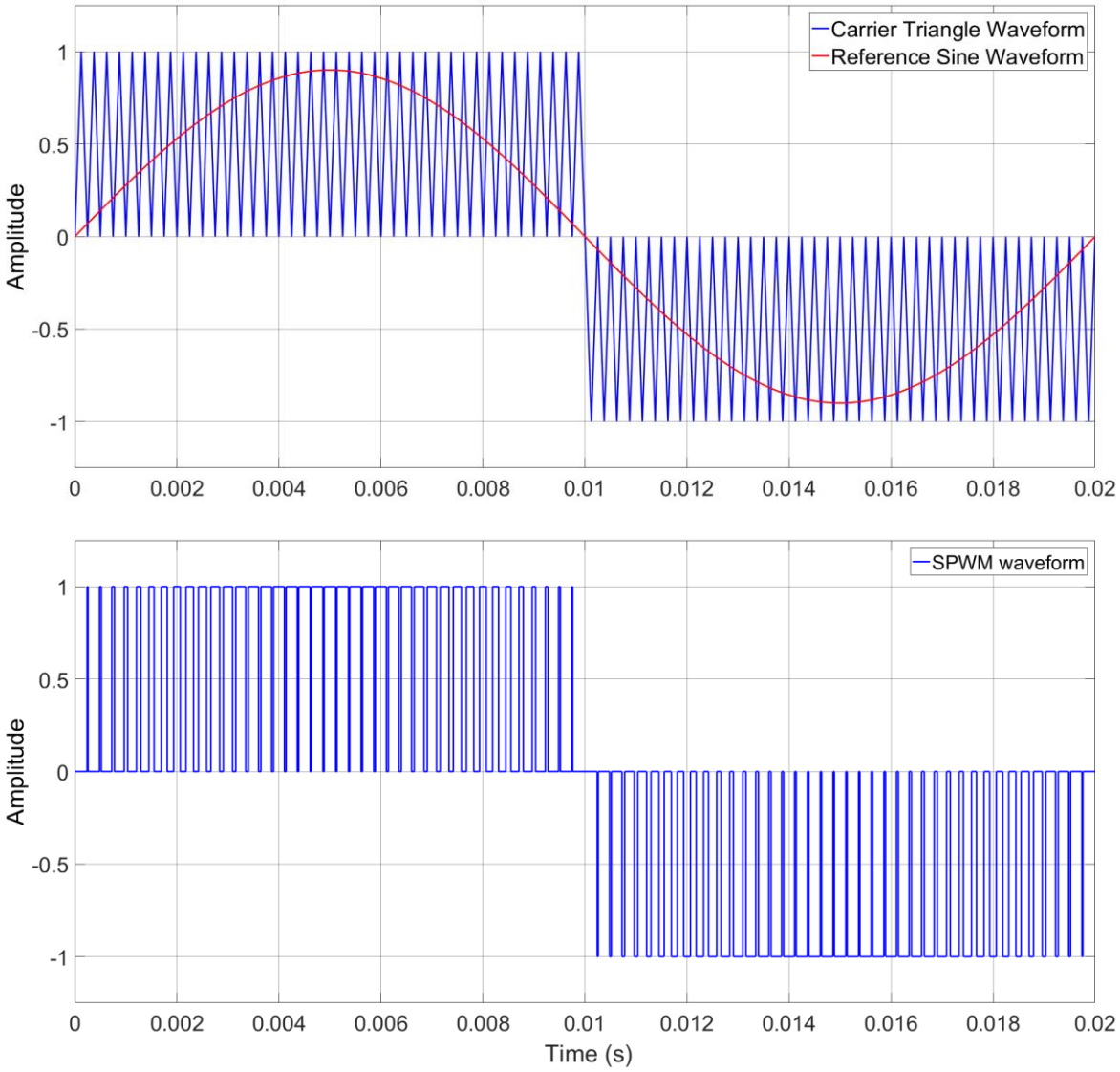

Figure 4.1: Inverter output waveform before filtering at 4kHz (Illustration)

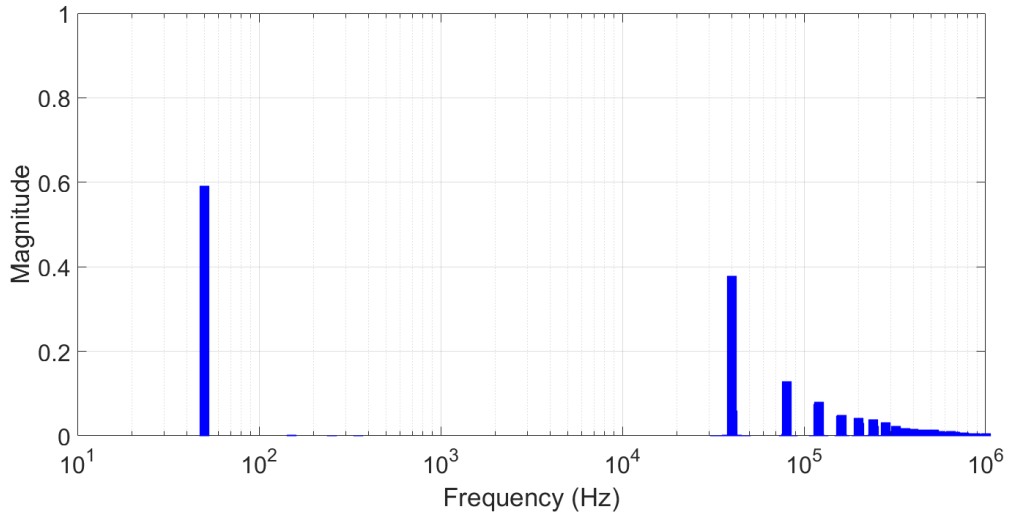

Figure 4.2: FFT analysis of the inverter waveform before filtering at 40kHz in 0.1s

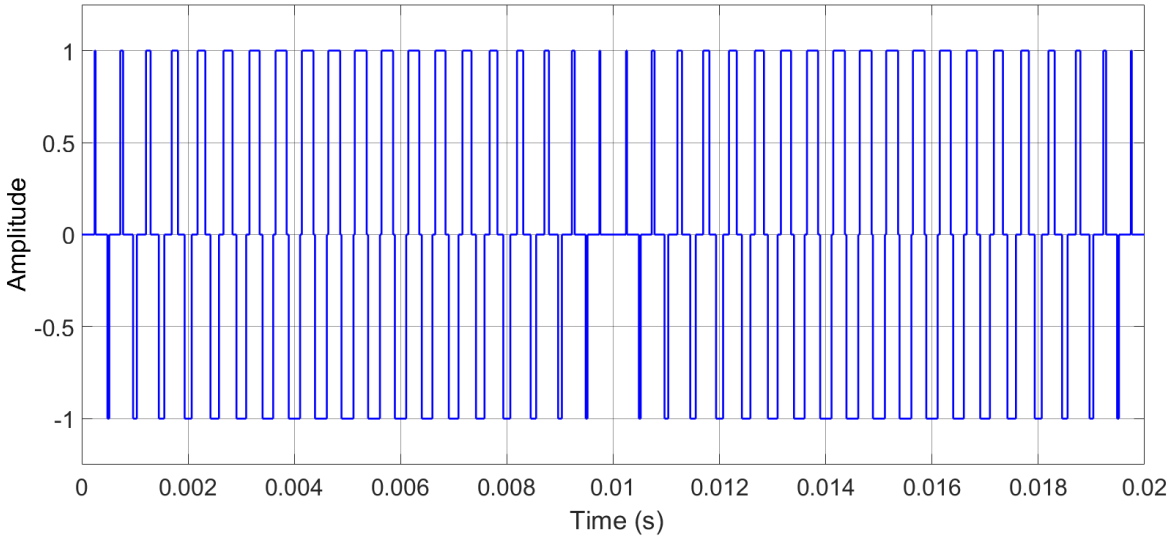

Figure 4.3: Waveform to pass through transformer at 4kHz (Illustration)

In Figure 4.3, the pulses of Figure 4.1 are flipped alternatively. By doing this, the frequency of waveform in Figure 4.1 changes to a much higher frequency one. Again, 4kHz in Figure 4.3 is for illustration purpose. The FFT response of the 40kHz waveform is shown Figure 4.4 below.

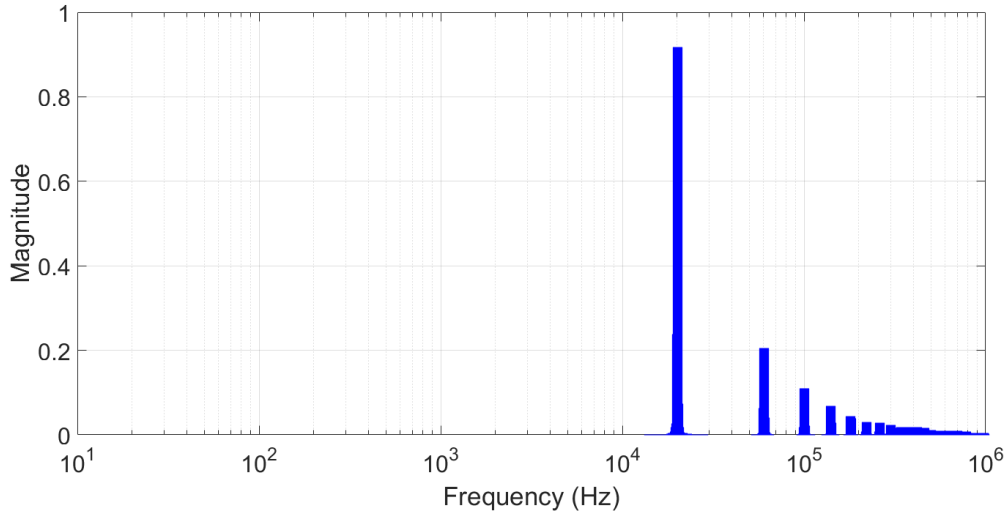

Figure 4.4: FFT analysis of waveform used for transformer at 40kHz in 0.1s

The amplitude component of the 50Hz is just 1.9497×10^{-6} and the main component is 0.9179 at 20kHz. Therefore, with a desire output waveform of 40kHz, the frequency pass through the transformer is half of it or 20kHz.

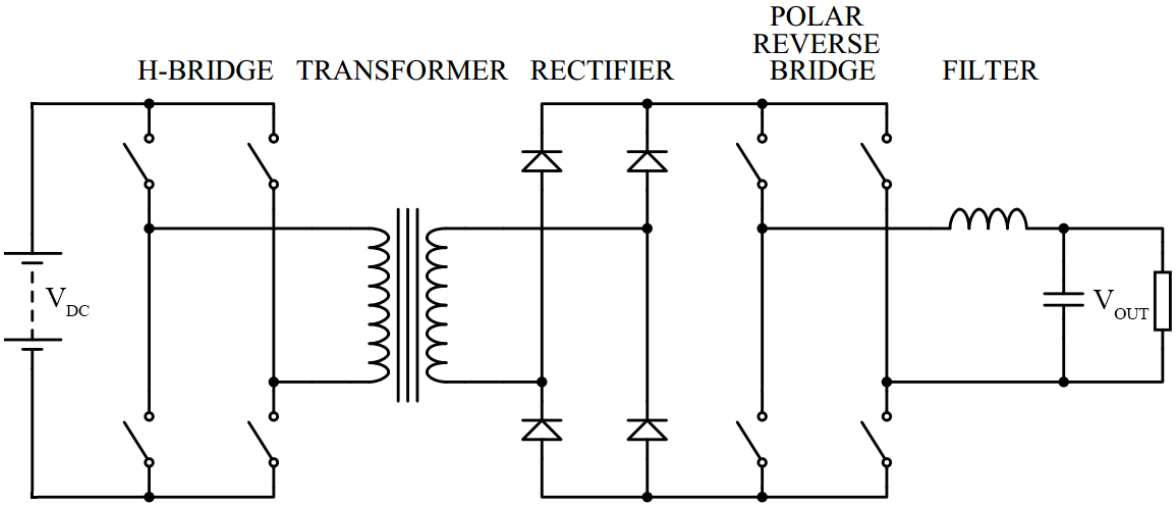

Figure 4.5: Schematic of DC/AC circuit

The final topology of DC/AC converter is shown in Figure 4.5. The first stage is H-bridge, which creates the high frequency PWM pulses. These pulses then pass through a transformer to boost the voltage to grid level. After that, a passive diode rectifier bridge is used to flip all pulses in negative side to positive side. There is no need to have an active rectifier because the current does not flow backward and the control is much simpler with the rectifier in comparison to an active switched rectifier. The next stage of the inverter is the polar reverse bridge to flip pulses at the frequency of 50Hz. And the final stage is LC filter which blocks all high frequency components and just let the fundamental frequency signal or 50Hz sinusoidal wave pass through. The passive LC filter is selected for its simplicity and it does not need to be controlled by the microcontroller.

The 400V is the amplitude of the carrier waveform of the SPWM method. The 400V square PWM waveform is then filtered by LC filter and outputs the pure sine wave of 230VAC. According to the distribution code, the highest grid voltage is 230VAC+10% or 253VAC. This means the peak voltage of grid is 358V. Therefore, a 400V carrier waveform is chosen.

The illustration of the waveform at stages of DC/AC topology is shown from Figure 4.6 to Figure 4.9 below.

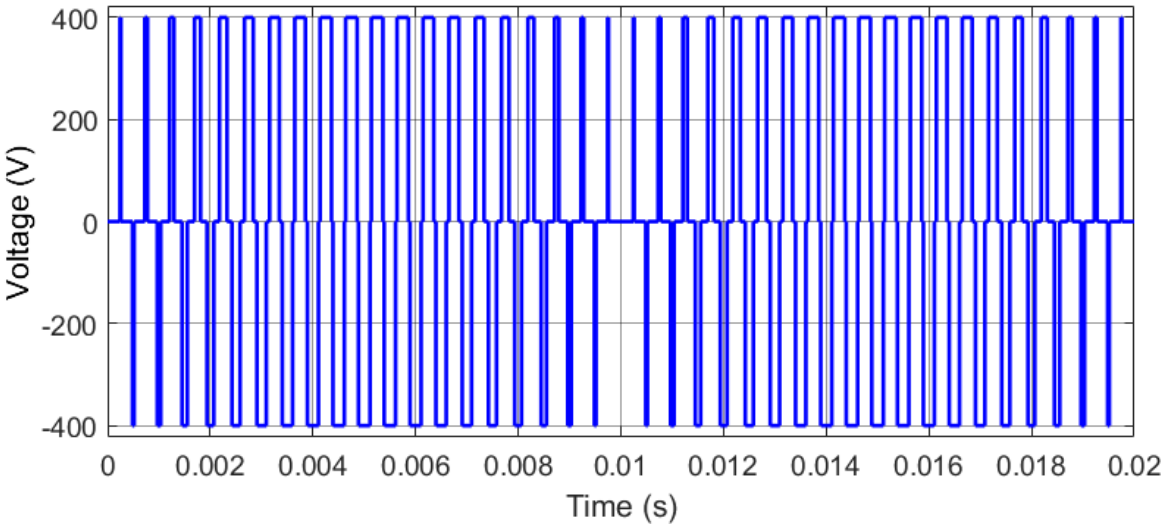

Figure 4.6: Output voltage of transformer

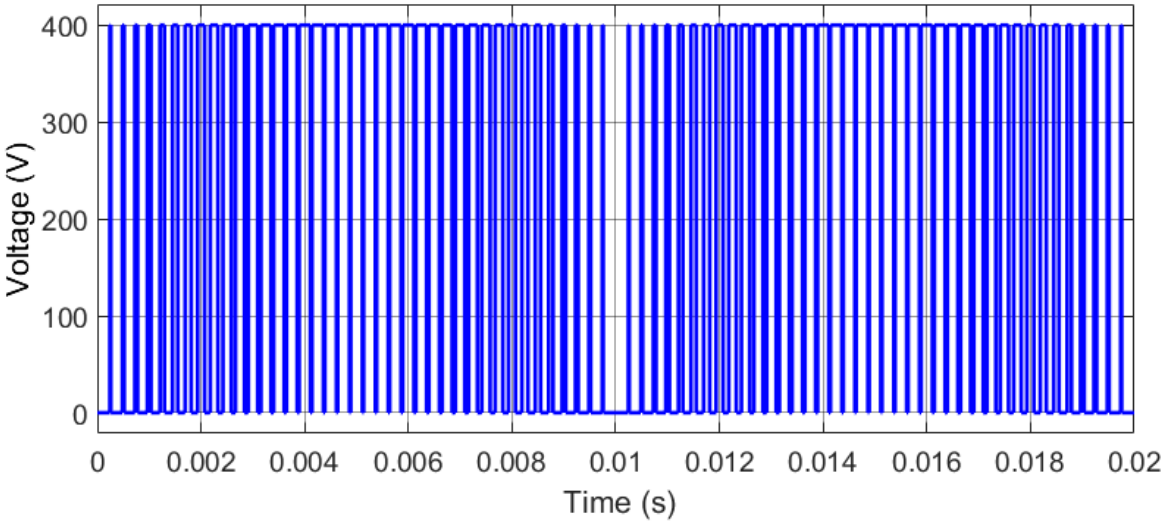

Figure 4.7: Output voltage of rectifier

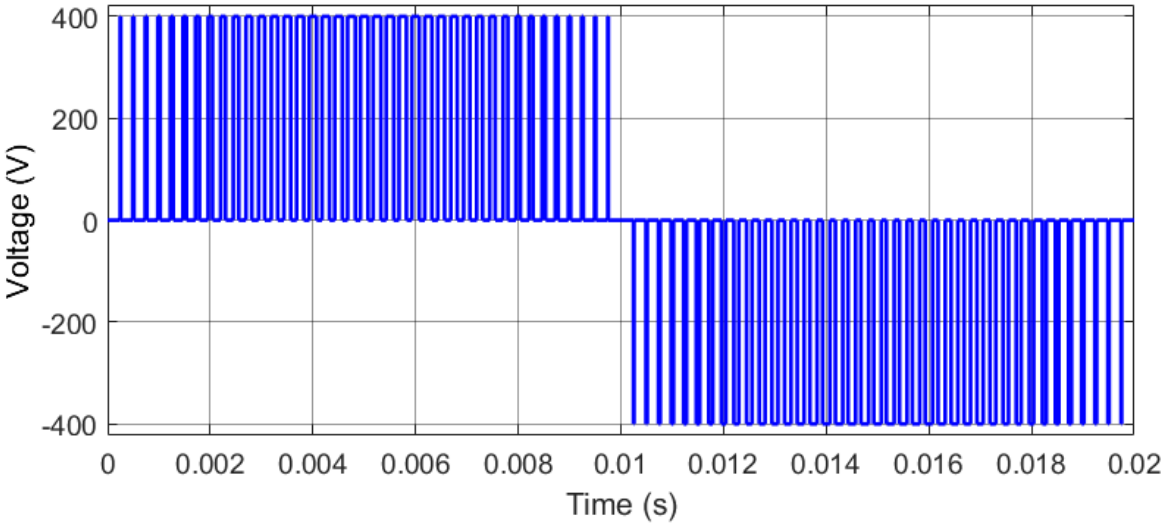

Figure 4.8: Output voltage of polar reverse bridge

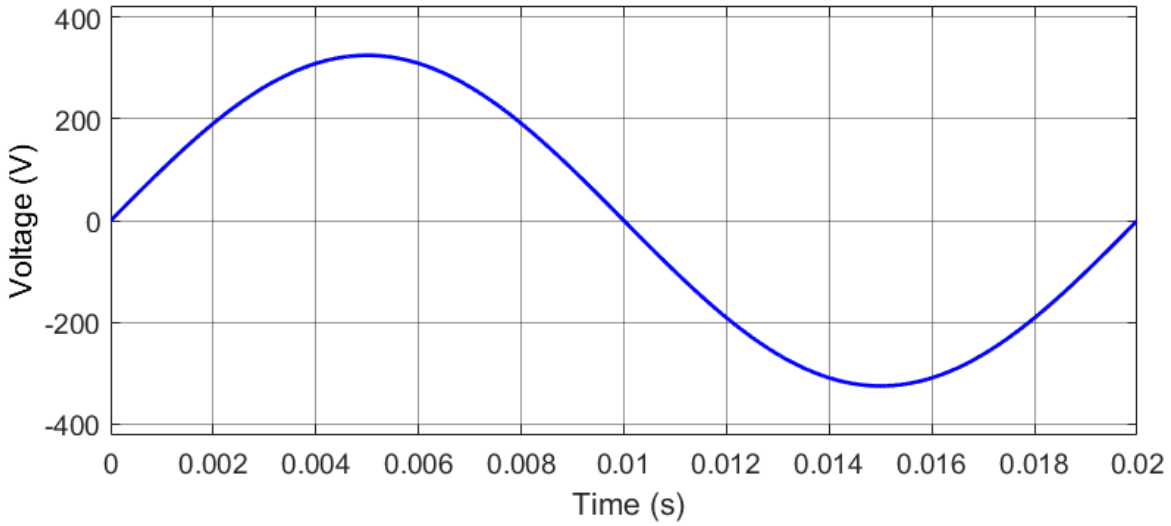

Figure 4.9: Output voltage of filter

The topology of this DC/AC converter is simulated and characterized experimentally in sections 4.2 and 4.5.

4.1.2. Power control theory

The output of the inverter will pass through an LC filter before connecting to grid. Let the grid voltage and current be $\boldsymbol{V}_{grid}$ and $\boldsymbol{I}_{grid}$, respectively. Also, let $\boldsymbol{V}_{inv}$ and $\boldsymbol{I}_{inv}$ be the fundamental voltage and current of the inverter before the filter, respectively. A model for studying power transfer can be built as shown in the figure below.

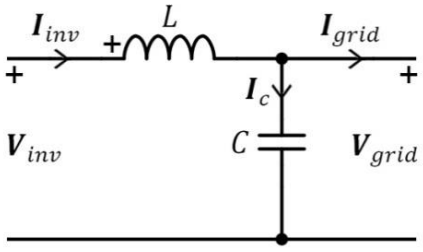

Figure 4.10: Power transfer model

The capacitor current $\boldsymbol{I}_c$ and inductor voltage $\boldsymbol{V}_L$ are calculated as:

$$\boldsymbol{I}_c = jC\omega\boldsymbol{V}_{grid} \tag{4.1}$$

$$\boldsymbol{V}_L = jL\omega\boldsymbol{I}_{inv} \tag{4.2}$$

Let δ be the angle between $\boldsymbol{V}_{grid}$ and $\boldsymbol{V}_{inv}$ as the following figure.

$$\boldsymbol{V}_{grid} = V_{grid}\angle 0° \tag{4.3}$$

$$\boldsymbol{V}_{inv} = V_{inv}\angle\delta = V_{inv}(\cos\delta + j\sin\delta) \tag{4.4}$$

Using Kirchhoff's voltage and current laws of the circuit, so:

$$\boldsymbol{I}_{inv} = \boldsymbol{I}_c + \boldsymbol{I}_{grid} \tag{4.5}$$

$$\boldsymbol{V}_{inv} = \boldsymbol{V}_L + \boldsymbol{V}_{grid} \tag{4.6}$$

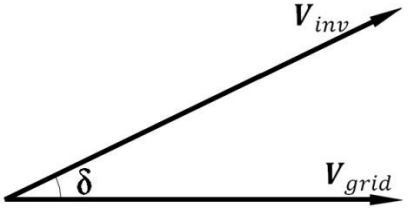

Figure 4.11: Phasor diagram between grid and inverter voltage

Therefore, the grid current $\boldsymbol{I}_{grid}$ can be calculated from the above equations as:

$$\boldsymbol{I}_{grid} = \frac{V_{inv}\sin\delta}{L\omega} - j\left(\frac{V_{inv}\cos\delta}{L\omega} + V_{grid}\left(C\omega - \frac{1}{L\omega}\right)\right) \tag{4.7}$$

The complex output power of the grid is:

$$\boldsymbol{S} = \frac{1}{2}\boldsymbol{V}_{grid}\boldsymbol{I}^*_{grid} \tag{4.8}$$

or
$$\boldsymbol{S} = \frac{1}{2}V_{grid}\left(\frac{V_{inv}\sin\delta}{L\omega} + j\left(\frac{V_{inv}\cos\delta}{L\omega} + V_{grid}\left(C\omega - \frac{1}{L\omega}\right)\right)\right) \tag{4.9}$$

The active and reactive powers of the output to the grid are then calculated:

$$P = Re(\boldsymbol{S}) = \frac{V_{grid}V_{inv}\sin\delta}{2L\omega} \tag{4.10}$$

$$Q = Im(\boldsymbol{S}) = \frac{V_{grid}}{2}\left(\frac{V_{inv}\cos\delta}{L\omega} + V_{grid}\left(C\omega - \frac{1}{L\omega}\right)\right) \tag{4.11}$$

From the two equations above, the value of angle δ is determined as:

$$\sin\delta = \frac{2L\omega P}{V_{grid}V_{inv}} \tag{4.12}$$

$$\cos\delta = \frac{2L\omega Q}{V_{grid}V_{inv}} + \frac{V_{grid}L\omega}{V_{inv}}\left(\frac{1}{L\omega} - C\omega\right) \tag{4.13}$$

And with Pythagorean Theorem of:

$$\sin^2\delta + \cos^2\delta = 1 \tag{4.14}$$

The peak value of inverter output V_{inv} and the angle δ is then calculated.

$$V_{inv} = \frac{2L\omega}{V_{grid}}\sqrt{P^2 + \left(Q + \frac{V_{grid}^2}{2}\left(\frac{1}{L\omega} - C\omega\right)\right)^2} \tag{4.15}$$

and $$\delta = \sin^{-1}\left(\frac{2L\omega P}{V_{grid}V_{inv}}\right) \quad (4.16)$$

Hence, from equations (4.15) and (4.16) the amplitude and phase angle of the inverter can be calculated by grid amplitude V_{grid}, active power P and reactive power Q. The grid amplitude V_{grid} can be measured by the sensor at the inverter output. The active power P is the MPP taken from the solar panel through the DC/DC converter. The reactive Q is usually set to be zero and it is set in the case of supporting the grid.

4.2. Simulation

MATLAB model is used for simulating the DC/AC converter and verifying the controlling theory in section 4.1.2. The model is designed and shown in Figure 4.12 and values used for the simulation are listed in Table 4.1.

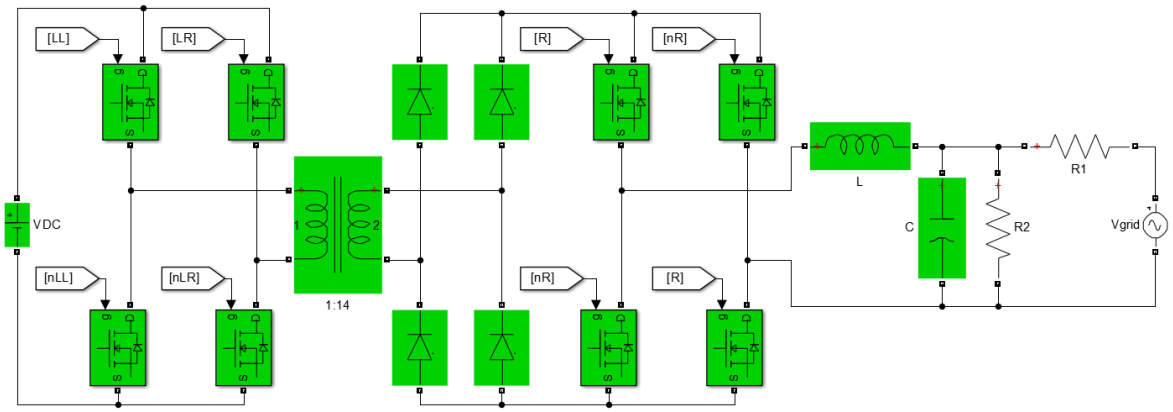

Figure 4.12: MATLAB simulation model DC/AC converter

P = 200W	Q = 20VAR
C = 0.1μF	L = 20mH
R_1 = 0.1Ω	R_2 = 10Ω
f_{grid} = 50Hz	$f_{H\text{-}bridge}$ = 40kHz
V_{DC} = 30VDC	V_{grid} = 230VAC (325.269V peak)

Table 4.1: Simulation values for inverter parameters

The inverter is set to output the active power of 200W and reactive power of 20VAR. The output of the inverter is connected to the grid of 230VAC and 50Hz. In the model, the H-bridge is controlled by signals LL and LR and the polar reverse bridge is switched by the signal R. These control signals are program to output the PWM based on the reference signal calculated from equations (4.15) and (4.16). From these equations the peak output of the inverter V_{inv} is calculated as 322.9823V and the phase angle δ is 1.384°.

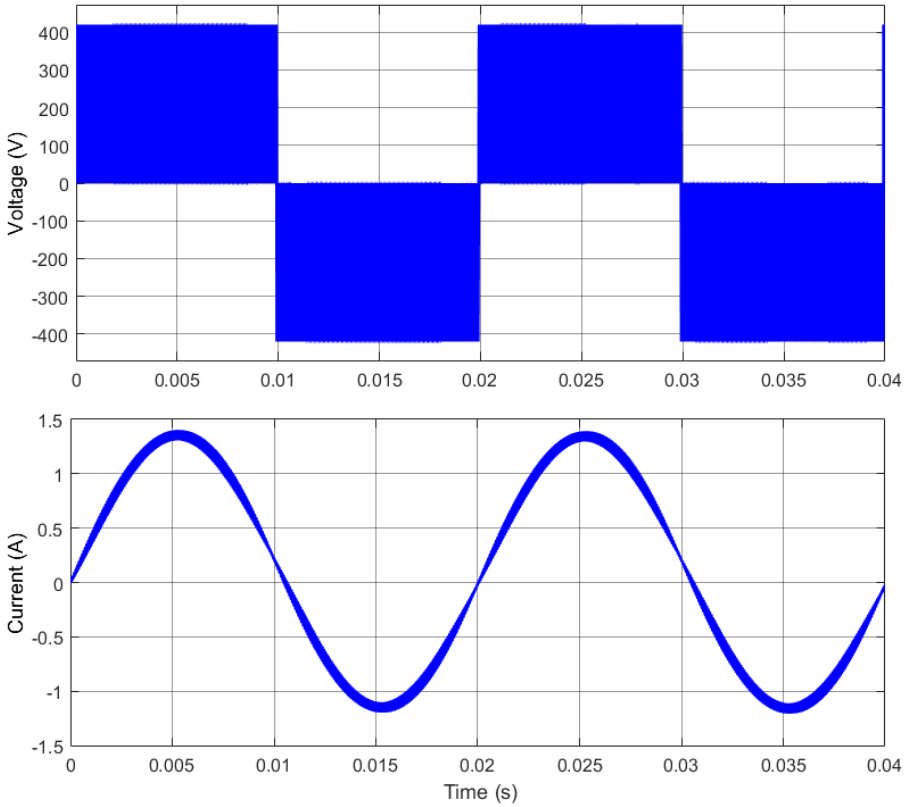

Figure 4.13: Simulated output voltage and current of polar reverse bridge

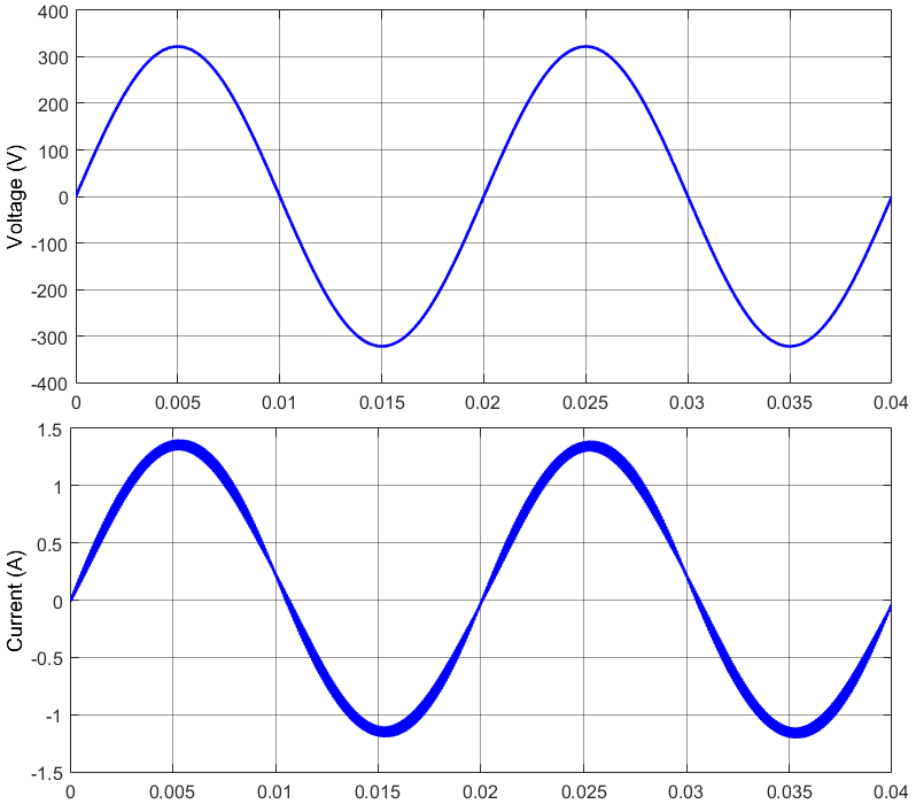

Figure 4.14: Simulated output voltage and current of filter

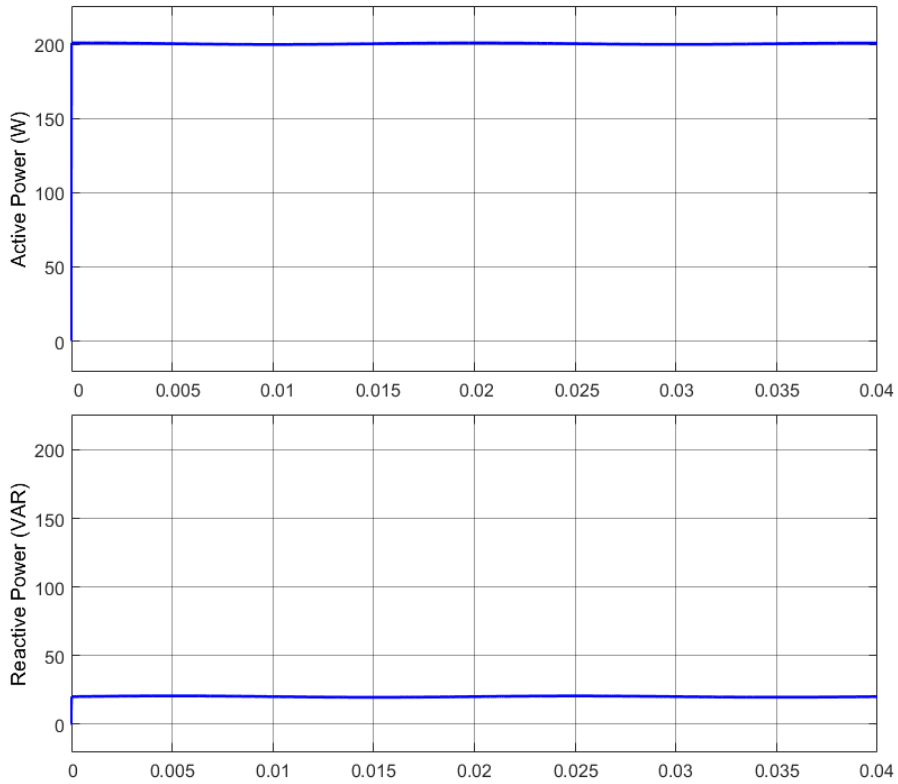

Figure 4.15: Simulated output active power and reactive power of inverter

From Figure 4.15, it can be seen that the output power of the inverter can be controlled by the phase and amplitude of the grid as shown in the equations (4.15) and (4.16).

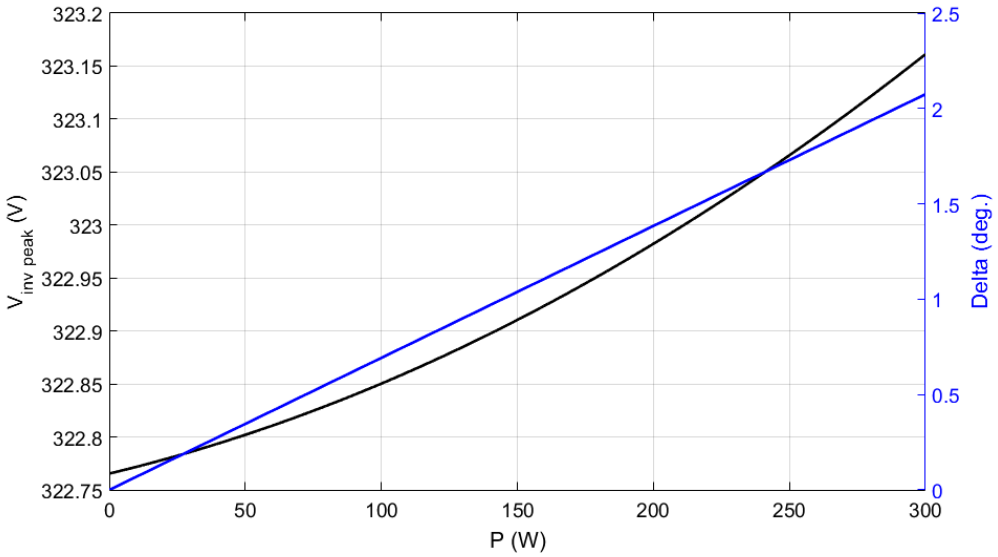

Figure 4.16: Inverter amplitude and phase angle versus output power

In Figure 4.16, the calculated amplitude V_{inv} and phase angle δ are calculated for different active power P values. It can be seen that the change in V_{inv} and δ are too small for every

1W increment of P. It is nearly impossible for the circuit and the microcontroller to calculate and output such these small changes. So that the controlling theory introduced in section 4.1.2 just works in the simulation and cannot be applied in practice.

4.3. Circuit board design

An experimental DC/AC circuit board is built for verification and shown in Figure 4.17. The H-bridge and polar reverse bridge consist of MOSFETs for switching. The four MOSFETs used for the first stage are IPA086N10N3 G power transistor and have the rating of 100V and 45A. The four transistors in the polar reverse bridge have the manufacturer part number of SiHF7N60E with the Drain-Source voltage of 650V and Continuous Drain current of 7A. Heat-sinks, which are put together with these transistors to release the heat and prevent the transistors from being too hot, are SW50-2 with thermal resistance of 8.6°C/W. For the rectifier, four 3A ultra-fast diodes are used. All above components can be bought in the market, except for the transformer and filter inductor, which are wound manually.

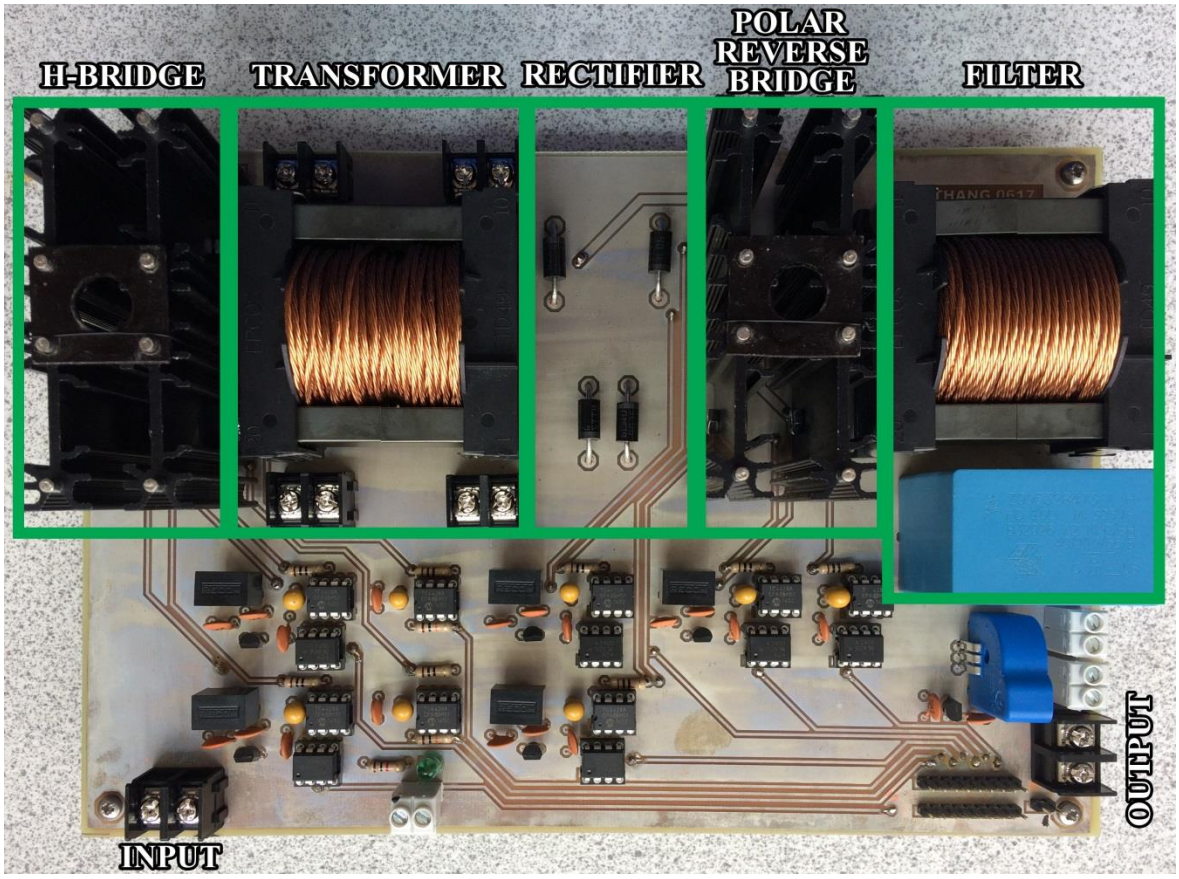

Figure 4.17: Laboratory prototype of DC/AC board

4.3.1. Transformer design

Similar to the design of inductors in the DC/DC section, the transformer needed to be designed for specific voltage ratings, input power, transformer ratio and frequency.

4.3.1.1. Methodology

In this section, a 2-coil transformer is considered. The purpose of re-building the formulas from the book [54] is that the Litz wire is used instead of a single conductor. Therefore, some steps, which do not affect the change of formulas, will be skipped. Moreover, same parameters, which are mentioned in the inductor design, will not be defined again in this section.

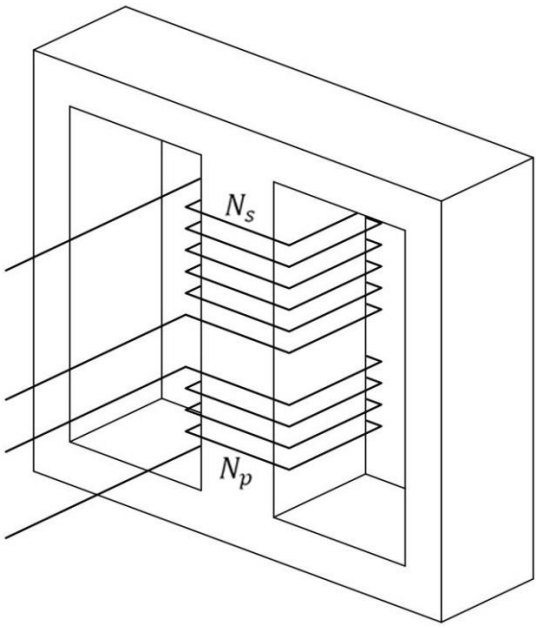

Figure 4.18: Basic E-core 2-coil transformer

General equations:

The equation below shows the input power P_{in} is related with elements which are mentioned in the inductor design section and the waveform factor k_v.

$$2P_{in} = f k_v k_u B_{max} A_p J_0 \tag{4.17}$$

The area of the winding A_w consists of the primary and secondary windings.

$$A_w = 9N_p n_{Litz\_p} A_{strand\_p} + 9N_s n_{Litz\_s} A_{strand\_s} = k_u A_{wd} \tag{4.18}$$

Power loss:

The power loss of the wire consists with two parts of primary and secondary sides.

$$P_{wire} = R_{wire\_p} I_{rms\_p}^2 + R_{wire\_s} I_{rms\_s}^2 \tag{4.19}$$

or $$P_{wire} = \rho l_{turn}\left(\frac{N_p I_{rms\_p}^2}{7n_{Litz\_p}A_{strand\_s}} + \frac{N_s I_{rms\_s}^2}{7n_{Litz\_s}A_{strand\_s}}\right) \quad (4.20)$$

Current density J_0 is equal in both primary and secondary sides, so:

$$J_0 = \frac{I_{rms\_p}}{7n_{Litz\_p}A_{strand\_p}} = \frac{I_{rms\_s}}{7n_{Litz\_s}A_{strand\_s}} \quad (4.21)$$

Combine the equations (4.18), (4.20) and (4.21), the power loss of the winding is:

$$P_{wire} = 7\rho l_{turn}J_0^2\left(n_{Litz\_p}A_{strand\_p}N_p + n_{Litz\_s}A_{strand\_s}N_s\right) \quad (4.22)$$

or $$P_{wire} = \frac{7}{9}\rho l_{turn}J_0^2 k_u A_{wd} \quad (4.23)$$

With volume of the winding is

$$V_w = l_{turn}A_{wd} \quad (4.24)$$

So combine (4.23) and (4.24), the power loss of the winding P_{wire} is then:

$$P_{wire} = \frac{7}{9}\rho V_w k_u J_0^2 \quad (4.25)$$

The total loss in the transformer is defined as in equations (3.76) and (3.77) with $\gamma = 1$.

$$P_{loss} = h_c A_t \Delta T = 2P_{wire} \quad (4.26)$$

so $$h_c A_t \Delta T = \frac{14}{9}\rho V_w k_u J_0^2 \quad (4.27)$$

Calculating current density:

Thus, from equation (4.27), the current density J_0 of transformer is calculated as:

$$J_0 = \sqrt{\frac{9h_c A_t \Delta T}{14\rho V_w k_u}} \quad (4.28)$$

With A_t, V_w and k_t are defined in the equations below.

$$A_t = k_a A_p^{1/2} \quad (4.29)$$

$$V_w = k_w A_p^{3/4} \quad (4.30)$$

and $$k_t = \sqrt{\frac{h_c k_a}{\rho k_w}} \quad (4.31)$$

Then the current density J_0 from equation (4.28) is:

$$J_0 = k_t\sqrt{\frac{9\Delta T}{14k_u}}\frac{1}{\sqrt[8]{A_p}} \quad (4.32)$$

Calculating transformer size:

From equations (4.17) and (4.32), A_p is calculated as follows:

$$A_p = \left(\frac{2P_{in}}{f k_t k_v B_{max}} \sqrt{\frac{14}{9 k_u \Delta T}} \right)^{\frac{8}{7}} \tag{4.33}$$

Calculating optimum flux density:

The following equation is used for calculating the optimum flux density B_o:

$$\left(\frac{P_{loss}}{2} \right)^{\frac{2}{3}} = P_{wire}^{\frac{1}{12}} P_{core}^{\frac{7}{12}} \tag{4.34}$$

Where P_{core} is the core loss and is similar to the equation (3.94). Taken $\beta = 2$, the core loss is then calculated by the optimum flux density B_o as:

$$P_{core} = V_c k_{core} f^{\alpha} B_o^{\beta} = V_c k_{core} f^{\alpha} B_o^2 \tag{4.35}$$

Hence, combining three equations (4.25), (4.26) and (4.35) to equation (4.34):

$$\left(\frac{h_c A_t \Delta T}{2} \right)^{\frac{2}{3}} = \left(\frac{7}{9} \rho k_w A_p^{\frac{3}{4}} k_u J_0^2 \right)^{\frac{1}{12}} \left(k_c A_p^{\frac{3}{4}} k_{core} f^{\alpha} B_o^2 \right)^{\frac{7}{12}} \tag{4.36}$$

or

$$\left(\frac{h_c k_a \Delta T}{2} \right)^{\frac{2}{3}} = \left(\frac{7}{9} \rho k_w k_u \right)^{\frac{1}{12}} (k_c k_{core} f^{\alpha} B_o^2)^{\frac{7}{12}} (A_p J_0)^{\frac{1}{6}} \tag{4.37}$$

Taken $A_p J_0$ from equation (4.17), then:

$$A_p J_0 = \frac{2P_{in}}{f k_v k_u B_o} \tag{4.38}$$

After that, substitute $A_p J_0$ from equation (4.38) to (4.37), the value of B_o is calculated.

$$B_o = \frac{\left(\frac{1}{2} h_c k_a \Delta T \right)^{\frac{2}{3}}}{\left(\frac{7}{9} \rho k_w k_u \right)^{\frac{1}{12}} (k_c k_{core} f^{\alpha})^{\frac{7}{12}} \left(\frac{2P_{in}}{f k_v k_u} \right)^{\frac{1}{6}}} \tag{4.39}$$

The value of optimum flux density B_o should not be larger than the saturation value B_{sat}.

Calculating winding turns:

Finally, the number of primary winding turns is determined as the formula below.

$$N_p = \frac{V_{rms\_p}}{2 k_v f B_o A_c} \tag{4.40}$$

The value of secondary turns N_s will be calculated through N_p and the transformer ratio.

4.3.1.2. Calculation for the transformer

Similar to calculating inductor, a ferrite core is chosen for this application. The transformer is used to boost the low voltage of battery to grid level. Then the initial values needed for calculating are listed in the following table.

f = 20kHz	k_u = 0.5	ΔT = 30°C
P_{in} = 280W	k_v = 4	T_{max} = 70°C
V_{rms_p} = 33.6V	$N_s/N_p = 14$	B_{sat} = 0.2T

Table 4.2: Initial values for calculating transformer

First from (4.39), the optimum flux density is calculated.

$$B_o = \frac{\left(\frac{1}{2}\times 10\times 40\times 30\right)^{\frac{2}{3}}}{\left(\frac{7}{9}(2.06\times 10^{-8})\times 10\times 0.5\right)^{\frac{1}{12}}(5.6\times 16.9\times 20000^{1.25})^{\frac{7}{12}}\left(\frac{2\times 280}{20000\times 4\times 0.5}\right)^{\frac{1}{6}}} = 0.135\text{T} \quad (4.41)$$

The value of B_o is less than the saturation flux density B_{sat} of ferrite core, then the next step is carried out. The core size is determined from equation (4.33) as follows.

$$A_p = \left(\frac{2\times 280}{20000\times(48.2\times 10^3)\times 4\times 0.13}\sqrt{\frac{14}{9\times 0.5\times 30}}\right)^{\frac{8}{7}} = 4.14\text{cm}^4 \quad (4.42)$$

Choose the core ETD49 which has the A_{p_ETD49} = 5.8cm^4. Specifications of the coil are based on the Table 3.8. From equation (4.40), the number of primary turns is calculated as below:

$$N_p = \frac{33.6}{2\times 4\times 20000\times 0.13\times(2.11\times 10^{-4})} = 7.4 \quad (4.43)$$

Choose N_p = 8 turns. With the ratio of 14, therefore N_s = 112 turns. The core loss of the transformer is calculated from equation (4.35).

$$P_{core} = (2.41\times 10^{-5})\times 16.9\times 20000^{1.25}0.135^2 = 1.76\text{W} \quad (4.44)$$

The current density is calculated from equation (4.32):

$$J_0 = (48.2\times 10^3)\sqrt{\frac{9\times 30}{14\times 0.5}}\frac{1}{\sqrt[8]{(5.8\times 10^{-8})}} = 2.4\text{A/mm}^2 \quad (4.45)$$

The power loss of the winding is taken from equation (4.23) and the value of ρ is the same as in equation (3.98):

$$P_{wire} = \frac{7}{9}(2.06\times 10^{-8})\times 0.087\times(2.4\times 10^6)^2\times 0.5\times(2.75\times 10^{-4}) = 0.66\text{W} \quad (4.46)$$

Therefore, the total power loss of the transformer is then:

$$P_{loss} = P_{core} + P_{wire} = 1.76 + 0.66 = 2.42\text{W} \quad (4.47)$$

After winding, the measured inductance of the primary side is 0.272mH and the inductance of the secondary side is 53.6mH. Similar to the equation (3.111), the core size using Litz wires is 15% smaller than the core size using a single conductor.

4.3.2. Grid measuring

To synchronize to the grid, the frequency, phase and amplitude values need to be determined. To measure the grid values, a small transformer is used to step down the high voltage of grid to the lower level for the microcontroller.

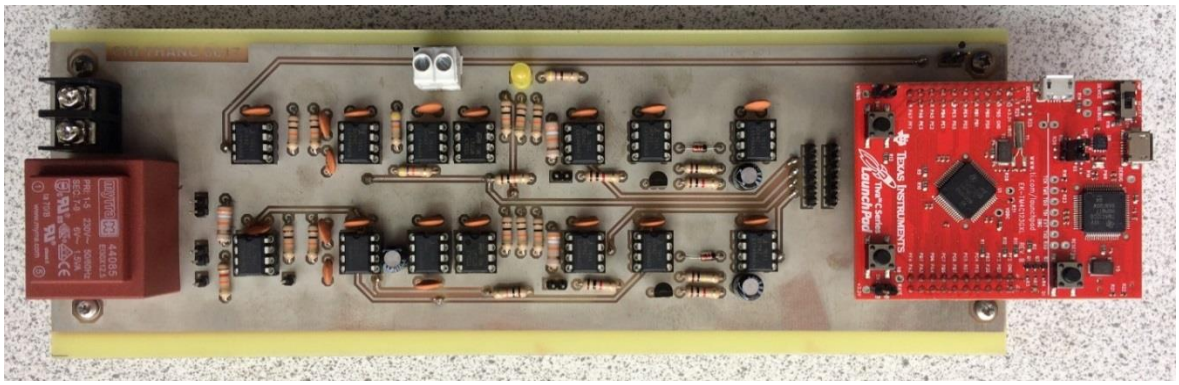

Figure 4.19: Laboratory prototype of grid sensing board

Because the input grid voltage is bipolar, 5V and -5V power supplies are needed for the op-amps to operate. The 5V power supply can be taken from the DC/DC board. To get -5V supply from 5V, a voltage converter ICL7660 is used.

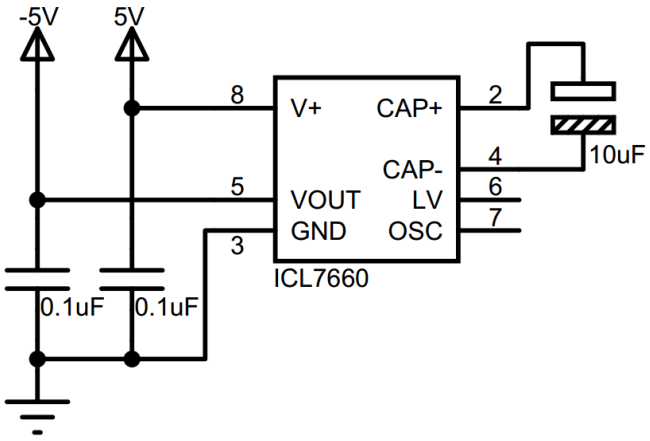

Figure 4.20: ICL7660 circuit of -5V supply

In this research, a peak detector is used for capturing the grid voltage amplitude and a zero-crossing detector (ZCD) is used for measuring the grid frequency and phase. However, both detectors depend on the grid quantities, which contain not only the fundamental component, but also a lot of harmonics. An active low-pass filter (LPF) is therefore required to remove all harmonics.

4.3.2.1. Grid filtering

An active filter is a good choice in comparison with a passive filter in signal conditioning applications. A 2nd-order Sallen-Key Low-pass-filter [62] was selected for the system under consideration.

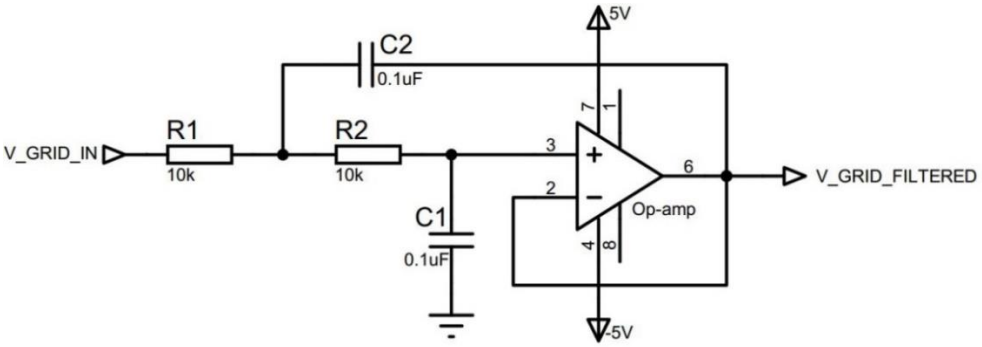

Figure 4.21: Schematic circuit of 2nd-order Sallen-Key Low-pass-filter [62]

The cut-off frequency f_c of this filter is:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} = \frac{1}{2\pi RC} \tag{4.48}$$

In the design, the resistor and capacitor values are equal or $R_1 = R_2 = R$ and $C_1 = C_2 = C$. With the chosen capacitors of 0.1µF and the cut-off frequency of 150Hz, the resistor value is then calculated as 10kΩ. With the selected values, the transfer function of this filter is:

$$H(s) = \frac{\frac{1}{R^2C^2}}{s^2 + \frac{2}{RC}s + \frac{1}{R^2C^2}} = \frac{1000000}{s^2 + 2000s + 1000000} \tag{4.49}$$

The Bode diagram of the transfer function is shown in Figure 4.22.

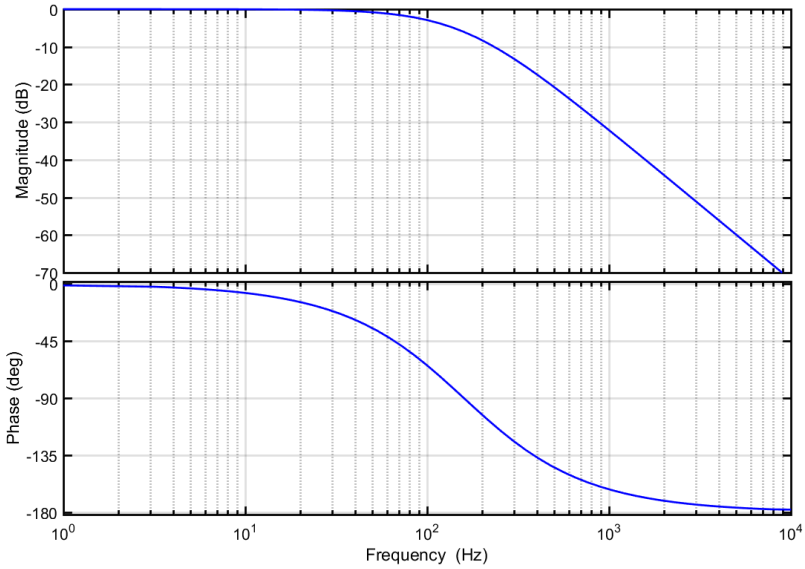

Figure 4.22: Bode diagram of the active filter

The filter can get rid of high frequency noise but it causes the signal to be delayed. The phase delay at the frequency 50Hz is calculated as 34.88° or 1.94ms. This value is verified by the experiment with a hardware circuit.

4.3.2.2. Grid zero-crossing detector

The circuit for the ZCD is simple and does not consist of many components. The grid signal will be compared to the zero level or ground. A voltage comparator LM311 is selected for this task.

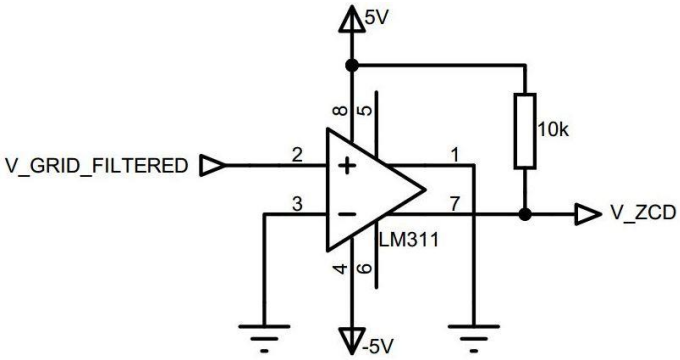

Figure 4.23: Schematic circuit of ZCD

The output of ZCD is 5V when the grid voltage is positive and is zero when grid is negative. By this, the phase and the frequency of grid can be read by the microcontroller.

4.3.2.3. Grid peak detector

The amplitude of grid may vary because of the load, so that it needs to be checked every cycle. The following Figure 4.24 shows the circuit to measure the grid peak value.

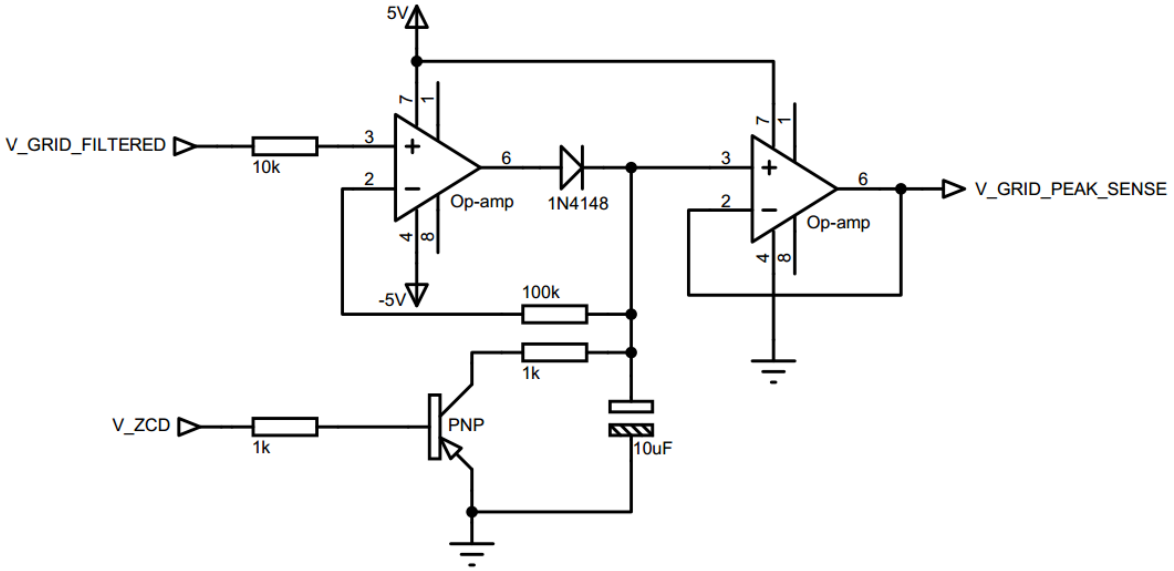

Figure 4.24: Schematic circuit of peak detector

An electrolytic capacitor is used to store the maximum value of the input of every cycle. After storing the peak value in one cycle, the capacitor needs to be discharged for the next cycle. Therefore, a small PNP transistor is placed in parallel with the capacitor for this task. The output of ZCD is utilized to switch the transistor on and off. By this way, the microcontroller requires one less PWM channel and the programming is easier.

4.3.3. MOSFET gate driver

The controlling PWM signals are generated by the microcontroller. The design of the low-side driver is similar to the one of DC/DC converter circuit. The challenge of this part is to design a high-side MOSFET driver.

The optocoupler HCPL-2400 is used. Its output is inverted, so that the output of the optocoupler is connected to the inverting driver of TC4428.

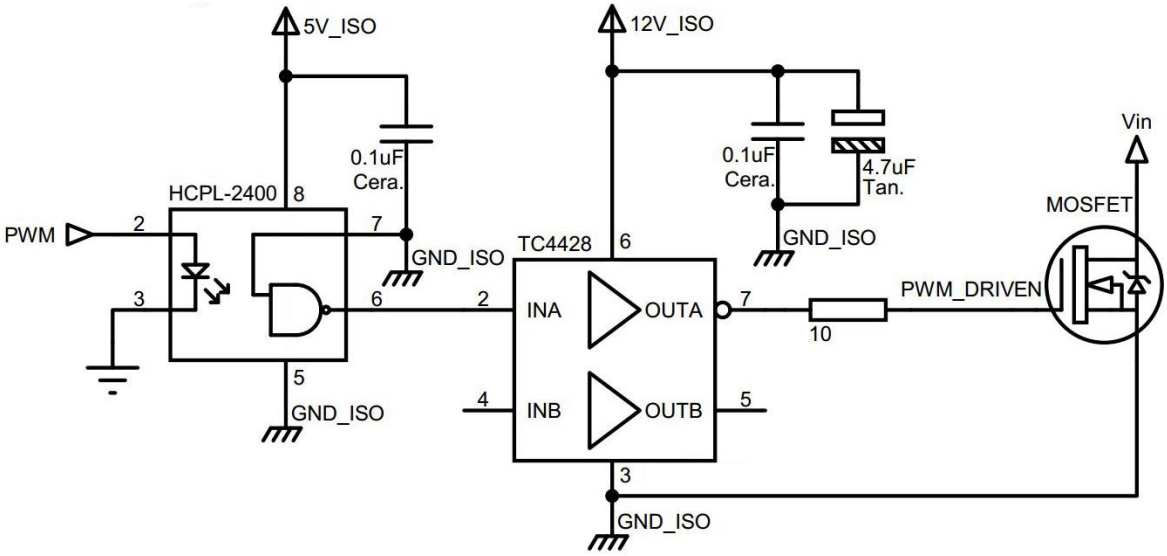

Figure 4.25: Schematic of high-side MOSFET driver

For the high-side driver circuit, not only the input signals but also the power supplies need to be isolated. The converter RI-1212S is used for converting 12V input to isolated 12V output.

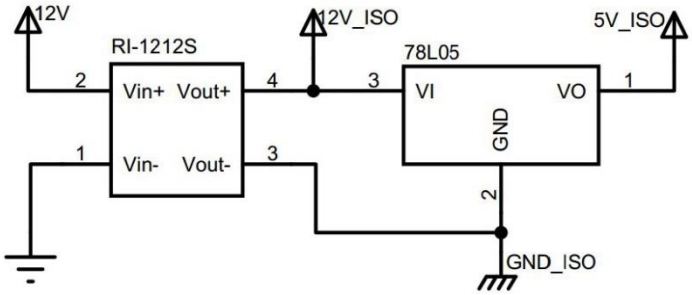

Figure 4.26: Schematic of isolated 5V&12V supplies for MOSFET driver

The isolated 5V supply is taken from a linear converter 78L05 because this power supply is just used for the optocoupler. The HCPL-2400 current load is 4mA, so that the power loss in the 78L05 is about 28mW which is acceptable.

4.4. Programming

There are H-bridge and polar reverse bridges in the circuit, therefore two PWM modules 0 and 1 are used. The PWM signals in the H-bridge are at 40kHz while the signals in the polar reverse bridge are at 50Hz.

4.4.1. SPWM generating

There are many methods to generate the SPWM to the H-bridge. The first way is using the analog generators by comparing a reference sinusoidal wave to a triangular one. This way requires a lot of components and has noise.

The other way is using a digital method to calculate the sine values by the microcontroller. However, getting sine values in the microcontroller requires many calculating cycles and the microcontroller needs to work harder and longer for every switching cycle.

A simple digital way to get the SPWM output is a look-up table. In this method, values of sine are pre-calculated and stored in a table. For the switching frequency of 40kHz and the grid output frequency of 50Hz, there are 800 sine values for every cycle of 20ms. Because the sine wave is symmetric, a half of these values or 400 points are enough for generating the whole cycle.

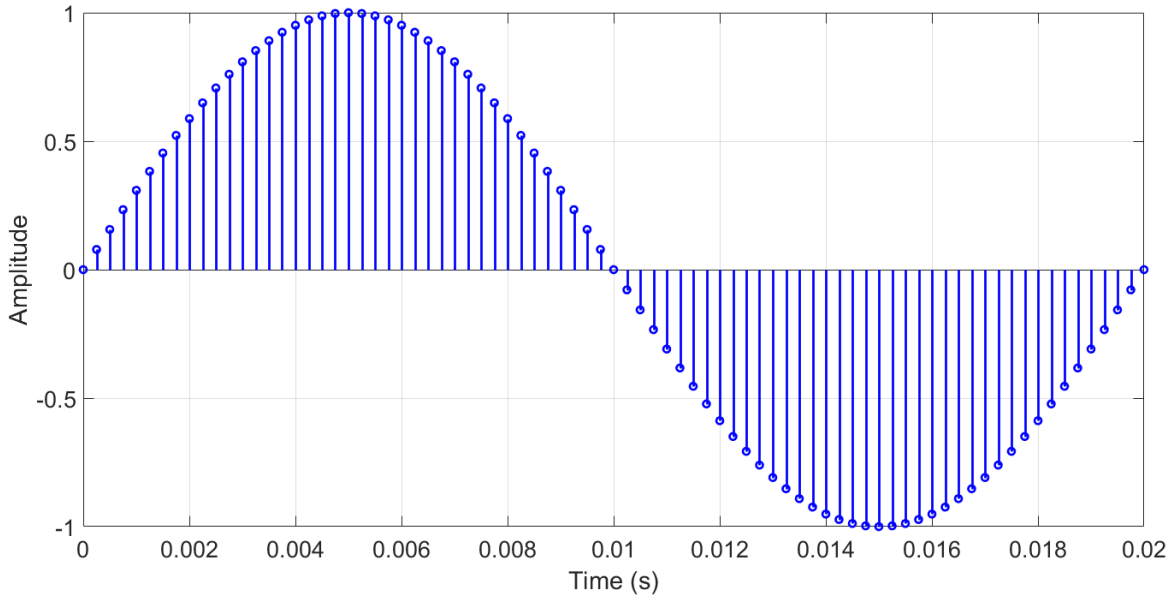

Figure 4.27: Example of 50Hz sine values with sampling of 4kHz

4.4.2. Frequency control

Because the grid frequency is not fixed and may vary around 50Hz, the output PWM should be adapted to the grid frequency. The distribution code for transmission systems states that the frequency of normal operation ranges from 49.8Hz to 50.2Hz [48]. Therefore, by adding or removing a few points in the peak of the sine waveform, the frequency may be controllable. It is nearly flat at the peak of the sinusoidal waveform and adding or subtracting a few points there does not affect the shape of the output.

At the peak values of frequency or 49.8Hz and 50.2Hz, the algorithm will add or minus at maximum 4 points for every cycle.

4.4.3. Phase control

Figure 4.28 shows the time delay of the ZCD output with respect to the grid voltage. The time difference from the falling-edge of the ZCD signal to the grid is 8ms, which is shown in Figure 4.31.

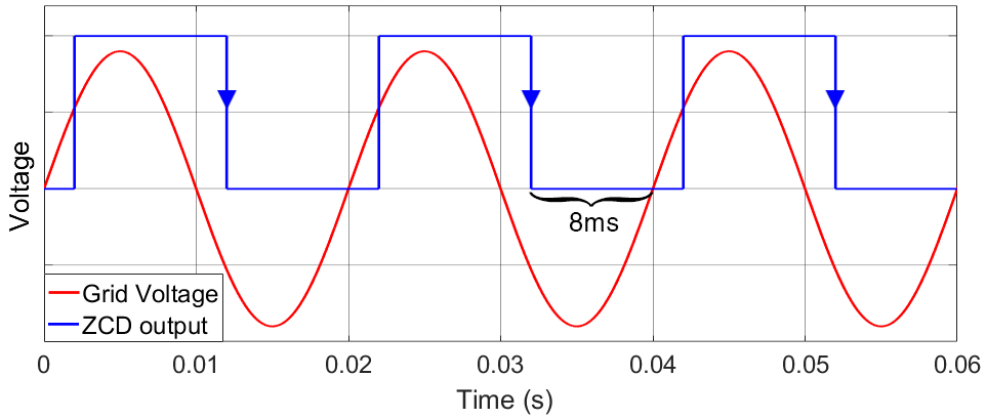

Figure 4.28: ZCD signal and grid voltage

To synchronize the grid with the ZCD input, the output of the PWM needs to be delayed by the program. For the switching of 40kHz frequency or 25μs period, the program will delay 320 cycles or 8ms for synchronizing to the grid.

4.4.4. Operation

The flowchart of the programming is shown in Figure 4.29. The signals of LL, LR and R are the PWM output to control the MOSFETs as shown in Figure 4.12. There are two interrupts in the coding which are the 40kHz PWM timer and the falling-edge of the ZCD signal.

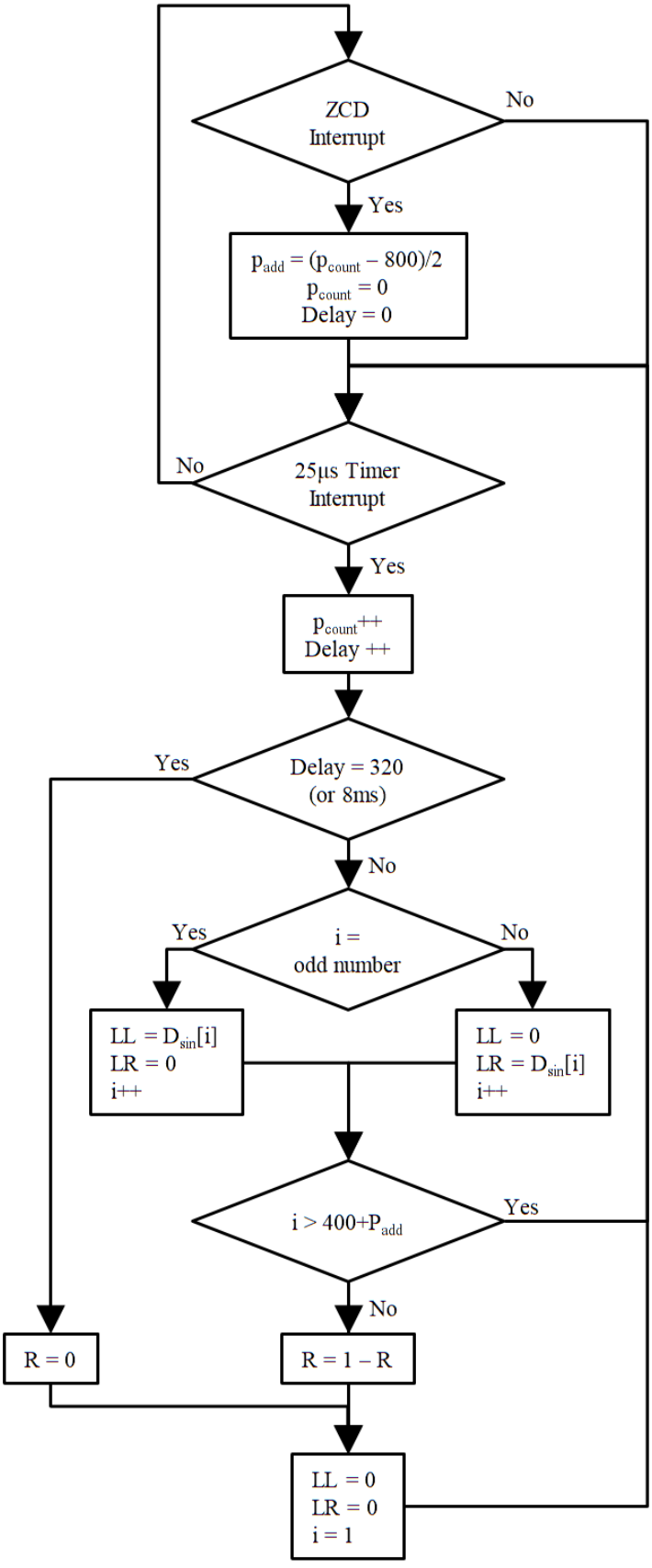

Figure 4.29: Simple flowchart of inverter programming

The 40kHz PWM interrupt is used to update the duty cycle values for controlling the switches. The values of LL and LR are determined by an array D_{sin} pre-calculated and stored in the microcontroller memory. Because the output waveform of the H-bridge is at high frequency, LL and LR are updated alternately or LL is updated duty cycle while LR is turned off and vice versa.

The ZCD interrupt occurs when the falling-edge of the signal is detected by the microcontroller. This interrupt is used for counting the period of the grid, the counted point p_{count} is set to be zero when the ZCD interrupt happens. Then p_{count} is incremented in each 25μs period and should be 800 with a standard grid frequency of 50Hz.

The controlling signal R is used for switching the Polar Reverse Bridge at 50Hz therefore it does not need to be updated as fast as the LL and LR. The updating frequency of R is the same as the ZCD interrupt.

In the flowchart in Figure 4.29, the ADC of grid peak is not mentioned because the output voltage of the inverter is controlled manually. The detail program is shown in the Appendix.

4.5. Experimental results

The designed circuit is built to verify the prototype and the coding. In the experiment, the transformer, low-side and high-side gate drivers are evaluated. The sensor circuit is also tested before experimenting with the inverter.

The connection of the experiment is shown in Figure 4.30. Instead of connecting to the grid, the output of the inverter is connected to a resistor.

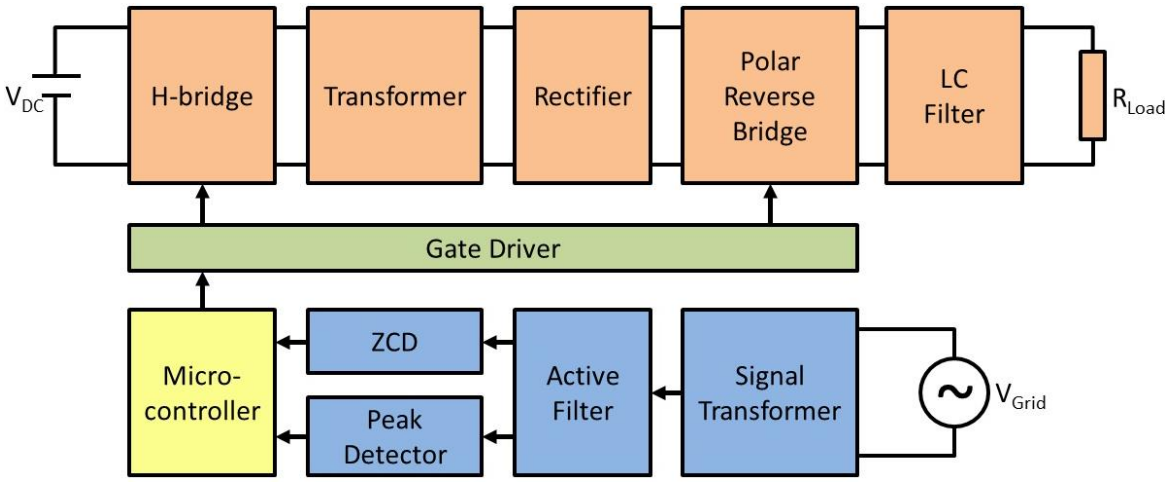

Figure 4.30: Block connection of the experiment

Grid voltage is connected to the sensor circuit for measuring the frequency and amplitude of the grid. The outputs of the sensors are then read by a microcontroller. After that, the microcontroller outputs the PWM signals to the gate-driver circuits to drive the MOSFETs of the H-bridge and polar reverse bridge.

4.5.1. Grid measuring

The grid measurement is important for the coding and synchronizing of the inverter. The sensor circuit includes ZCD, peak detector and filter, which were calibrated and measured to compensate the delay time and peak ratio data for the programming.

4.5.1.1. Grid filtering

As mentioned previously, a small transformer is used for decreasing the grid voltage. The output of the transformer is then passed through an active filter to get rid of unexpected noise and harmonic spectrums. This is important because the accuracy of the sensor depends on the quality of the input signal. Figure 4.31 below shows the grid voltage and the filtered signal from the transformer.

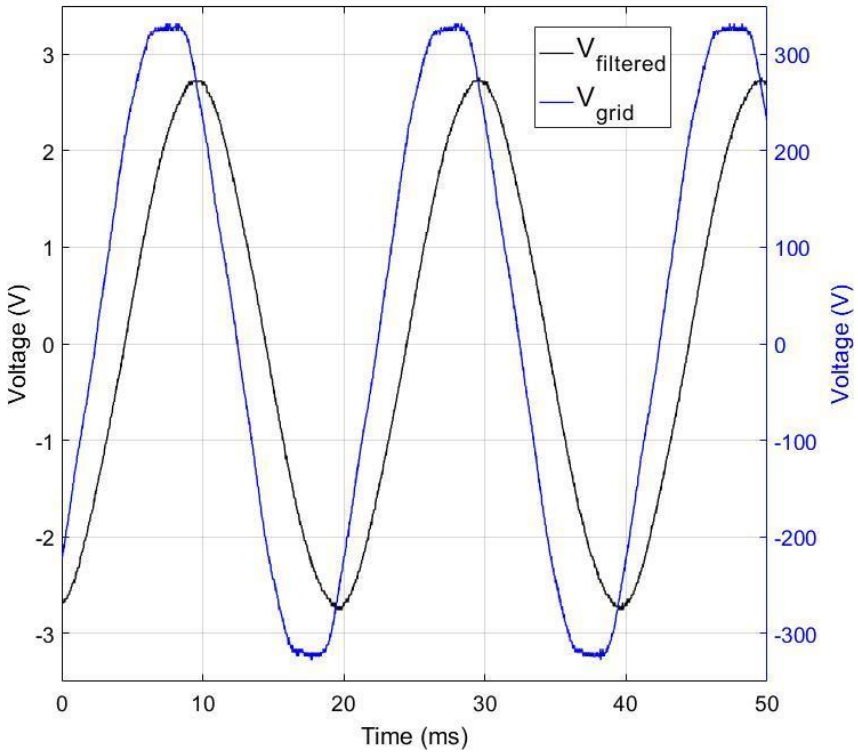

Figure 4.31: Grid voltage and grid filtered signal

The output of the signal transformer has the phase leading the grid voltage, and it is measured of 0.4ms. The theory calculation of the phase lag of the filter is 1.94ms as

mentioned in 4.3.2.1. So the phase lag of the filtered signal to the grid is 1.54ms. The measured phase lag of the filtered signal to the grid voltage is 2ms. The difference of the calculated value to the measure one is 0.46ms which is caused by the tolerance of component values. The phase-shifted value is used for the programming.

4.5.1.2. Grid zero-crossing detector

The circuit design and the output of the ZCD are simple, but this signal is very important for controlling both the frequency and phase angle of the grid. As can be seen in Figure 4.32, the output voltage of the ZCD immediately change from zero to a higher level when the input signal changes from negative to positive values. By measuring the time between two consecutive falling-edges of ZCD signals, the period of the grid can be collected. Moreover, the rising-edge and falling edge also indicate the phase of the grid when it passes zero.

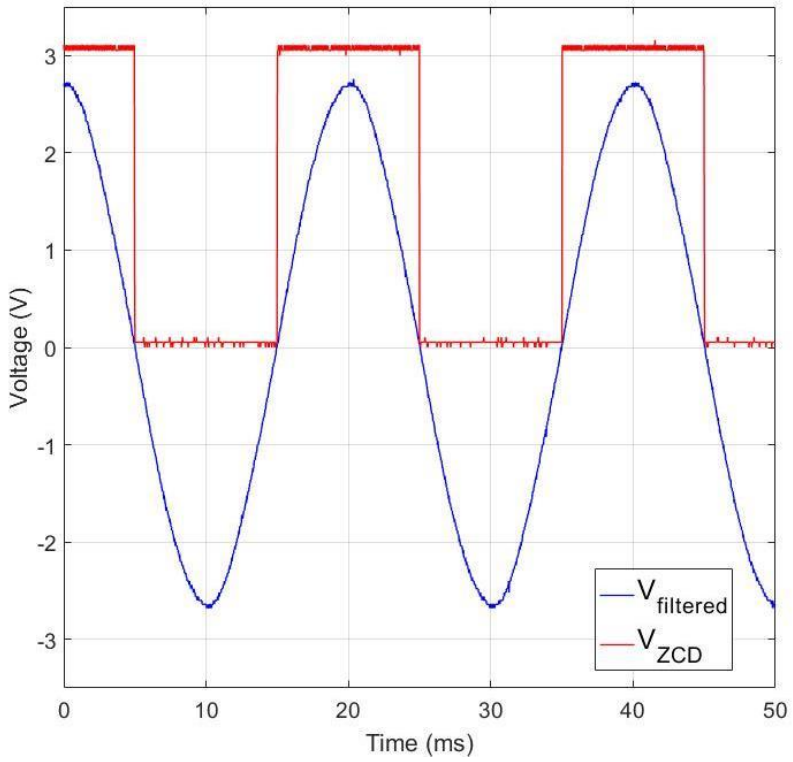

Figure 4.32: Zero-crossing detector output and grid filtered signal

4.5.1.3. Grid peak detector

The peak detector in section 4.3.2.3 stores the maximum input value to the capacitor and then discharges it for the next period. As seen in Figure 4.33, during half of the grid period, the output signal of the peak detector increases its level and maintains its highest value. In

the other half, the capacitor voltage drops slowly for refreshing to the next period. The maximum value of the input signal is kept unchanged for a quarter of the period till the falling-edge of the ZCD signal. Therefore, in the coding, the falling-edge interrupt is chosen instead of rising-edge.

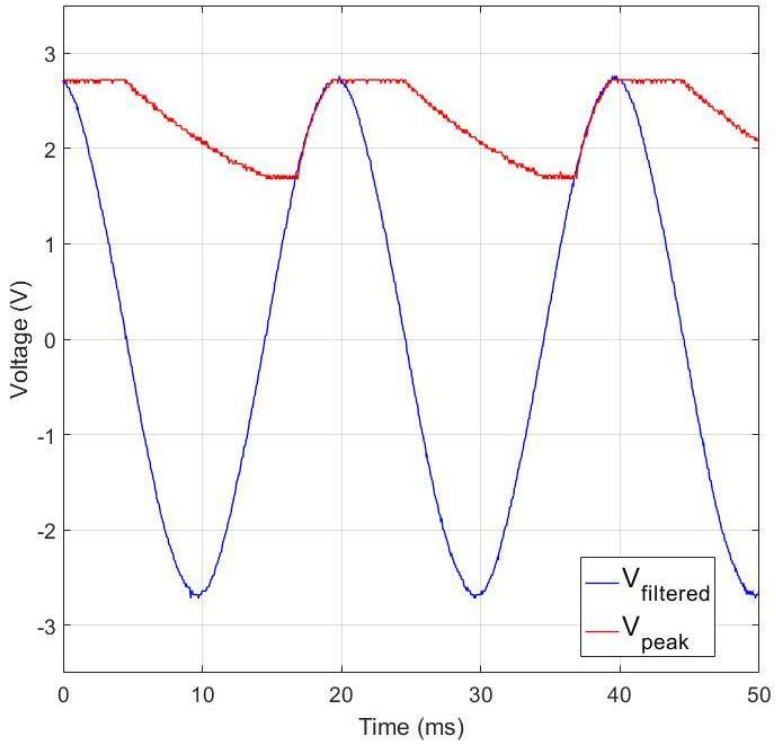

Figure 4.33: Peak detector output and grid filtered signal

4.5.2. DC/AC circuit

After testing the measuring sensors, the circuit performance is then experimentally measured. The input of the circuit is a 30VDC source and the output is connected to a 1.13kΩ resistor.

In Figure 4.34, the output of the transformer is shown and it is at 20kHz frequency. In a transformer, there are many parasitic parameters such as inter-winding capacitance, self-capacitance and winding resistance. The parasitic capacitance values are the cause of the ringing of the transformer waveform [63]. The winding of the transformer is made manually so that the effect of the parasitic values is high. The ripples and overshoot of this signal are nearly double the signal but after the LC filter, the output of the inverter is clear of high frequency harmonics and synchronized to the frequency and phase of the grid as shown in Figure 4.35.

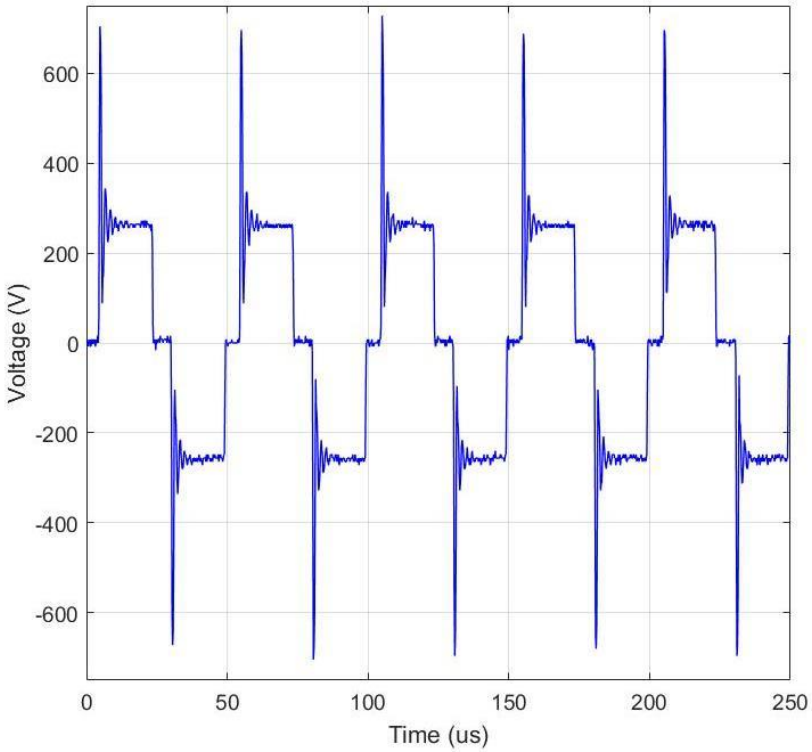

Figure 4.34: Experimental result of transformer output voltage

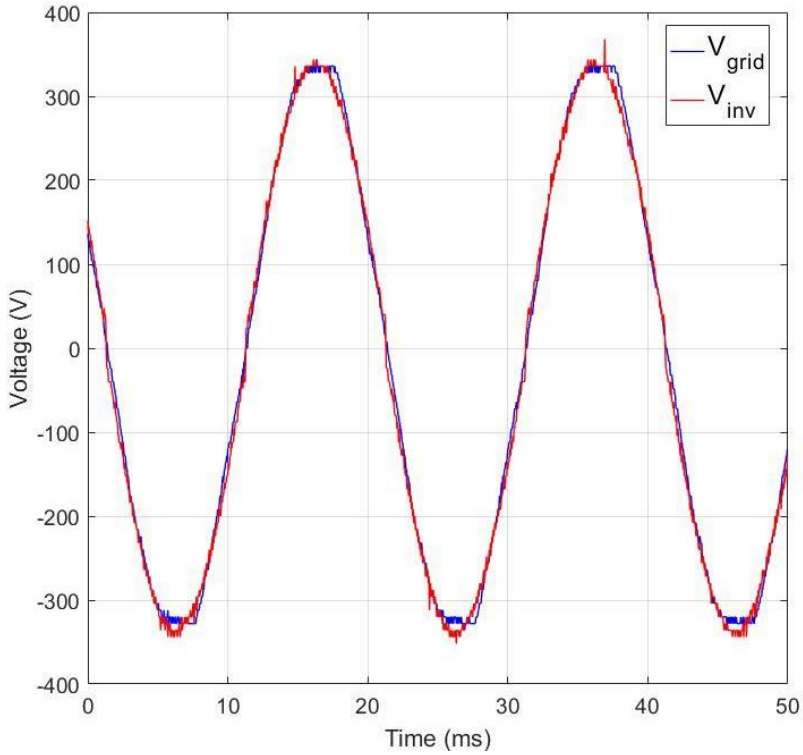

Figure 4.35: Experimental result of the inverter output

In the experiment, the inverter was not connected to the grid. In Figure 4.35, the grid voltage and the inverter output nearly match each other in amplitude, frequency and phase.

The circuit is built for verification purposes and this result has proven the topology of the DC/AC converter.

The output of the DC/AC converter was connected to a resistor. The connection between the inverter and the grid were not conducted. The output amplitude of the inverter was set manually because there were problems with the coding and gate driver circuit. The microcontroller worked with the interrupt input of ZCD and the inverter could export a sinusoidal output voltage which was synchronized to the grid frequency. The ADC module was supposed to read the data from the peak detector and updated every cycle of the grid frequency. However, when adding the ADC module to the programming code, one of the PWM output pins was broken by the feedback current of the gate driver circuit.

In conclusion, the DC/AC converter and the sensor circuits were tested for their performances. The experimental results were proven the topology of the DC/AC converter. The converter could export the output which was similar to the theory and the simulation. However, there were problems in coding and the implementation of the circuit which made the incompleteness of the experiment for the grid connection.

CHAPTER 5. CONCLUSION

In this section, the achievements, contributions and the successful work of this project are presented. In addition, during the time of the research, there were problems and difficulties in implementation and experiments. Proposed solutions for the problems and improvements are suggested in the future work.

5.1. Achievements

The research is to build a micro-inverter, which converts DC power from a solar module to supply AC grid power. A literature review has been carried out to select a suitable topology for the converter. The two-stage micro-inverter is chosen with a DC/DC converter, a DC/AC converter and a Li-ion battery in between.

The selected DC/DC converter is SEPIC and the formulas for its operation and theoretical waveform of each component were presented in detail. The hardware circuit designed in this research including sensors, power supplies, heat-sinks and MOSFET gate drivers are shown. The design of an inductor is described in depth in this research. The inductor is wound by Litz wires, which perform better than a single conductor. The core size of using Litz wires is calculated to be 15% smaller than the core size using single conductor. The implemented SEPIC is tested and the output results are similar to the theory which means that the circuit meets the design requirements and the continuous current conditions.

The SEPIC is then used for testing the effectiveness of a novel MPPT algorithm called BS-P&O. A modified P&O method is introduced and then used for comparison to the BS-P&O. The BS-P&O has been proven to perform better than the traditional P&O, INC and modified P&O methods in both simulation and experiment. The efficiency of the BS-P&O is measured to be 1% higher than the traditional methods. The response time for the sudden change in the environment of this novel algorithm is less than 0.2s, which has been proven in both simulation and experiment.

The second stage of the micro-inverter is a DC/AC converter, which is more complicated than the DC/DC converter. The topology is designed for both boosting the low input voltage to grid level and converting DC to AC at 50Hz. The converter topology and PWM control are selected for the use of a high frequency transformer. Similar to the inductor, the

design and winding of the transformer are introduced using Litz wires and the detailed construction formulas are presented in this research.

The design of grid measurements is also described from theory to practical hardware circuit. These sensors are able to detect the frequency, amplitude and phase of both grid current and voltage. The measurement sensors are implemented and tested with the utility grid and the output results are read by the microcontroller to control MOSFET switches through PWM signals.

In the simulation, the DC/AC converter is controlled and connected to the utility grid. In the simulated version, the converter is able to output a pure sinusoidal wave and synchronize to the grid. It can also transfer active power to the grid by applying the formulas to control the voltage amplitude and phase of the converter before filtering.

In the experiment, the hardware DC/AC circuit can produce a sinusoidal output that is able to synchronize to the grid frequency and phase.

5.2. Problems and future work

Physical connection of the inverter to the grid was not carried out in the experiment because of the time limit and safety requirements. The theory of controlling the converter voltage and phase to export both active and reactive powers is just applied for the simulation. In practice, the controlled voltage and phase variations for power level control are too small for the sensor to measure and the microcontroller to calculate. Therefore, the approach of current controlling will be applied for the future work. Moreover, the microcontroller programming is challenged because there are many things involved such as timers, interrupt, PWM and ADC modules. There are in total 9 PWM outputs and 8 ADC inputs of the microcontroller for controlling both DC/DC and DC/AC circuits. Therefore, the design of the inverter will be modified for more efficient code execution.

In the process, the DC/DC and DC/AC converters were tested separately without affecting the other and their combined operation has not yet been experimentally demonstrated. The effectiveness of the battery as a buffer between these converters will also be considered in the future.

The use of the battery limits the output voltage of DC/DC converter at a low level. This requires more components and makes the inverter circuit more complicated to design and control. More effective and simpler topologies with energy storage will be investigated in the future studies.

Lastly, the sensor and gate driver circuits need to be designed in a smaller size and with less noise by using surface-mount devices (SMD). The method of measuring the grid by ZCD, peak detector and current sensor may be changed by more powerful devices in the market.

PUBLICATIONS

Chi-Thang Phan-Tan and Nam Nguyen-Quang, "A P&O MPPT method for photovoltaic applications based on binary-searching," *2016 IEEE International Conference on Sustainable Energy Technologies (ICSET)*, Hanoi, 2016, pp. 78-82.

Chi-Thang Phan-Tan and Nam Nguyen-Quang, "A SEPIC-Based Single-Phase Grid-Connected Micro-Inverter for Photovoltaic Applications," *2015 International Symposium on Electrical and Electronics Engineering (ISEE2015)*, Ho Chi Minh city, Oct. 2015, pp. 540-549.

APPENDIX

Program for MPPT BS-P&O method

```
#include <stdint.h>
#include <stdbool.h>
#include <stdlib.h>
#include <stdio.h>
#include "inc/hw_memmap.h"
#include "inc/hw_gpio.h"
#include "inc/hw_types.h"
#include "inc/tm4c123gh6pm.h"
#include "driverlib/sysctl.h"
#include "driverlib/gpio.h"
#include "driverlib/pin_map.h"
#include "driverlib/interrupt.h"
#include "driverlib/debug.h"
#include "driverlib/adc.h"
#include "driverlib/pwm.h"
#include "driverlib/timer.h"

//********************Variables_[start]********************//
uint8_t eP = 2, eD = 1, time = 1;
uint16_t i = 0;
uint16_t volatile D = 500, dD, dD0 = 16;
uint32_t fSW, fSampling; ADC0value[8];
float I1, I2, V1, V2, P1, P2, Vo;
float V_d[300], D_d[300], P_d[300];
float dP1 = 1, dP2, dV, k1 = 1, k2;
//********************Variables_[end]********************//

//********************Main Code_[start]********************//
int main(void){
	//SysClkFreq = (400MHz/2)/10 = 20MHz
	SysCtlClockSet(SYSCTL_SYSDIV_10|SYSCTL_USE_PLL|SYSCTL_OSC_MAIN|SYSCTL_XTAL_16MHZ);

	//=====TIMER0A_[start]=====//
	SysCtlPeripheralEnable(SYSCTL_PERIPH_TIMER0); //Enable TIMER0
	TimerConfigure(TIMER0_BASE, TIMER_CFG_PERIODIC); //TIMER0
	fSampling = (SysCtlClockGet()/50); //50Hz = 0.02s
	TimerLoadSet(TIMER0_BASE, TIMER_A, fSampling); //TIMER0A-50Hz
	IntEnable(INT_TIMER0A); //TIMER0A
	TimerIntEnable(TIMER0_BASE, TIMER_TIMA_TIMEOUT); //TIMER0A
	IntMasterEnable();
	TimerEnable(TIMER0_BASE, TIMER_A); //TIMER0A
	//=====TIMER0A_[end]=====//

	//=====PWM_setup_[start]=====//
	//SEPIC_40kHz  M1PWM5-PF1
	SysCtlPWMClockSet(SYSCTL_PWMDIV_1); //20MHz/1=20MHz for PWM clock
	SysCtlPeripheralEnable(SYSCTL_PERIPH_PWM1); //PWM Module1

	//=====PortF=====//
	SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOF); //PortF
	GPIOPinTypePWM(GPIO_PORTF_BASE, GPIO_PIN_1); //PF1
	GPIOPinConfigure(GPIO_PF1_M1PWM5); //PF1[M1PWM5]
	fSW = (SysCtlClockGet()/40000); //40kHz switching
```

```
        //=====Module1=====//
        PWMGenConfigure(PWM1_BASE, PWM_GEN_2, PWM_GEN_MODE_DOWN); //GEN2_M1PWM5
        PWMGenPeriodSet(PWM1_BASE, PWM_GEN_2, fSW); //GEN2_M1PWM5_40kHz
        PWMPulseWidthSet(PWM1_BASE, PWM_OUT_5, fSW*D/1000); //M1PWM5, Duty
        PWMOutputState(PWM1_BASE, PWM_OUT_5_BIT, true); //M1PWM5
        PWMGenEnable(PWM1_BASE, PWM_GEN_2); //M1_GEN2
        //=====PWM_setup_[end]=====//

        //=====ADC setup [start]=====//
        //Ipv  AIN7-PD0 & Vpv  AIN6-PD1

        SysCtlPeripheralEnable(SYSCTL_PERIPH_ADC0); //ADC0

        //ADC0 = average of 64 samples
        ADCHardwareOversampleConfigure(ADC0_BASE, 64);

        //ADC0-Sequencer0-8 samples-use default trigger-highest priority
        ADCSequenceConfigure(ADC0_BASE, 0, ADC_TRIGGER_PROCESSOR, 0);

        //ADC0-Sequencer0-sample0-AIN7
        ADCSequenceStepConfigure(ADC0_BASE,0,0,ADC_CTL_CH7);
        //ADC0-Sequencer0-sample1-AIN7
        ADCSequenceStepConfigure(ADC0_BASE,0,1,ADC_CTL_CH7);
        //ADC0-Sequencer0-sample2-AIN7
        ADCSequenceStepConfigure(ADC0_BASE,0,2,ADC_CTL_CH7);
        //ADC0-Sequencer0-sample3-AIN7
        ADCSequenceStepConfigure(ADC0_BASE,0,3,ADC_CTL_CH7);
        //ADC0-Sequencer0-sample4-AIN7
        ADCSequenceStepConfigure(ADC0_BASE,0,4,ADC_CTL_CH7);
        //ADC0-Sequencer0-sample5-AIN7
        ADCSequenceStepConfigure(ADC0_BASE,0,5,ADC_CTL_CH7);
        //ADC0-Sequencer0-sample6-AIN6
        ADCSequenceStepConfigure(ADC0_BASE,0,6,ADC_CTL_CH6);
        //ADC0-Sequencer0-sample7-AIN6
        ADCSequenceStepConfigure(ADC0_BASE,0,7,ADC_CTL_CH6|ADC_CTL_IE|ADC_CTL_END);

        ADCSequenceEnable(ADC0_BASE,0); //Enable ADC0-Sequencer0
        //=====ADC setup [end]=====//
        while(1)
        {}
}
//********************Main Code [end]*******************//

//********************TIMER0 Interrupt [start]*******************//
void TIMER0_Int(void) {
        TimerIntClear(TIMER0_BASE, TIMER_TIMA_TIMEOUT); //Clear TIMER0 interrupt
        ADCIntClear(ADC0_BASE, 0); //ADC0-Sequencer0
        ADCProcessorTrigger(ADC0_BASE, 0); //ADC0-Sequencer0
        while(!ADCIntStatus(ADC0_BASE, 0, false)) //ADC0-Sequencer0
        {}
        ADCSequenceDataGet(ADC0_BASE, 0, ADC0value); //ADC0-Sequencer0

        I2 = (((ADC0value[0]+ADC0value[1]+ADC0value[2]+ADC0value[3]+
             ADC0value[4]+ADC0value[5])*3.3/(6*4095))*1.03 - 2.524)*9.6;
        V2 = ((ADC0value[6]+ADC0value[7])*3.3/(2*4095))*14.1;
        P2 = V2*I2;
```

```
        //=====Data reading [start]=====//
        //Data for 6s (0.02s * 300 = 6s)
        if (i < 300) {
              V_d[i] = V2;
              D_d[i] = D;
              P_d[i] = P2;
              i++;
        }
        //=====Data reading [end]=====//

        //=====MPPT BS-P&O [start]=====//
        if (time == 1) {
              V1 = V2;
              I1 = I2;
              P1 = P2;
              dD = dD0;
              D = D + dD;
              time = 2;
        }
        else {
              if ((D > 900) || (D < 100)) {
                    D = 500;
              }
              dP2 = P2 - P1;
              dV = V2 - V1;
              if ((dD == 2) && (abs(dP2) > eP)){
                    dD = dD0;
                    D = D + dD;
              }
              else {
                    k2 = dP2*dV;

                    if (((k2*k1) < 0) && (dD > 2)){
                          dD = dD/2;
                          D = D - ((k2 >= 0) - (k2 < 0))*dD;
                    }
                    else {
                          D = D - ((k2 >= 0) - (k2 < 0))*dD;
                    }
                    if (dD < eD) {
                          dD = 0;
                    }
              }
              k1 = k2;
              V1 = V2;
              P1 = P2;
              dP1 = dP2;
        }
        //=====MPPT BS-P&O [end]=====//

        PWMPulseWidthSet(PWM1_BASE, PWM_OUT_5, fSW*D/1000); //M1PWM5, Duty
}
//********************TIMER0 Interrupt [end]********************//
```

Program for DC/AC converter

```
#include <stdint.h>
#include <stdbool.h>
#include <stdlib.h>
#include <stdio.h>
#include "inc/hw_memmap.h"
#include "inc/hw_gpio.h"
#include "inc/hw_types.h"
#include "inc/tm4c123gh6pm.h"
#include "driverlib/sysctl.h"
#include "driverlib/gpio.h"
#include "driverlib/pin_map.h"
#include "driverlib/interrupt.h"
#include "driverlib/debug.h"
#include "driverlib/pwm.h"
#include "driverlib/adc.h"

//********************Variables [start]********************//
int8_t volatile halfadd = 0;
uint8_t volatile ll, lr;
uint16_t volatile Dr = 1, Dlr = 500, Dll = 500;
uint16_t volatile i = 0, period = 800, period_count = 0, delay = 0;
uint32_t freq;
float volatile ma;
uint16_t Dsin[205] =
      { 0,   8,  16,  24,  31,  39,  47,  55,  63,  71,  78,  86,
       94, 102, 110, 118, 125, 133, 141, 149, 156, 164, 172, 180,
      187, 195, 203, 210, 218, 226, 233, 241, 249, 256, 264, 271,
      279, 287, 294, 302, 309, 316, 324, 331, 339, 346, 353, 361,
      368, 375, 383, 390, 397, 404, 412, 419, 426, 433, 440, 447,
      454, 461, 468, 475, 482, 489, 495, 502, 509, 516, 522, 529,
      536, 542, 549, 556, 562, 569, 575, 581, 588, 594, 600, 607,
      613, 619, 625, 631, 637, 643, 649, 655, 661, 667, 673, 679,
      685, 690, 696, 702, 707, 713, 718, 724, 729, 734, 740, 745,
      750, 755, 760, 765, 771, 775, 780, 785, 790, 795, 800, 804,
      809, 814, 818, 823, 827, 831, 836, 840, 844, 849, 853, 857,
      861, 865, 869, 872, 876, 880, 884, 887, 891, 895, 898, 901,
      905, 908, 911, 915, 918, 921, 924, 927, 930, 933, 935, 938,
      941, 944, 946, 949, 951, 953, 956, 958, 960, 962, 965, 967,
      969, 971, 972, 974, 976, 978, 979, 981, 982, 984, 985, 986,
      988, 989, 990, 991, 992, 993, 994, 995, 996, 996, 997, 998,
      998, 998, 999, 999, 1000,1000,1000,1000,1000,1000,1000,1000,1000};
//********************Variables [end]********************//

//********************Main Code [start]********************//
int main(void) {
      SysCtlClockSet(SYSCTL_SYSDIV_5|SYSCTL_USE_PLL|SYSCTL_OSC_MAIN|SYSCTL_XTAL_16MHZ);

      //=====PWM setup [start]=====//
            /*H-bridge_40kHz
             *     Left   High M1PWM2-PA6     Low M1PWM3-PA7
             *     Right  High M1PWM6-PF2     Low M1PWM7-PF3
             *Polar Reverse Bridge_50Hz
             *     Left   High M0PWM0-PB6     Low M0PWM1-PB7
             *     Right  High M0PWM6-PC4     Low M0PWM7-PC5
             */
```

```
SysCtlPWMClockSet(SYSCTL_PWMDIV_1); // PWM clock = 20MHz/1 = 20MHz
SysCtlPeripheralEnable(SYSCTL_PERIPH_PWM0); //PWM Module0
SysCtlPeripheralEnable(SYSCTL_PERIPH_PWM1); //PWM Module1

      //-----PortA-----//
SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA); //PortA
GPIOPinTypePWM(GPIO_PORTA_BASE, GPIO_PIN_6|GPIO_PIN_7); //PA6-PA7
GPIOPinConfigure(GPIO_PA6_M1PWM2); //PA6[M1PWM2]
GPIOPinConfigure(GPIO_PA7_M1PWM3); //PA7[M1PWM3]
      //-----PortB-----//
SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOB); //PortB
GPIOPinTypePWM(GPIO_PORTB_BASE, GPIO_PIN_6|GPIO_PIN_7); //PB6-PB7
GPIOPinConfigure(GPIO_PB6_M0PWM0); //PB6[M0PWM0]
GPIOPinConfigure(GPIO_PB7_M0PWM1); //PB7[M0PWM1]
      //-----PortC-----//
SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOC); //PortC
GPIOPinTypePWM(GPIO_PORTC_BASE, GPIO_PIN_4|GPIO_PIN_5); //PC4-PC5
GPIOPinConfigure(GPIO_PC4_M0PWM6); //PC4[M0PWM6]
GPIOPinConfigure(GPIO_PC5_M0PWM7); //PC5[M0PWM7]
      //-----PortF-----//
SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOF); //PortF
GPIOPinTypePWM(GPIO_PORTF_BASE, GPIO_PIN_2|GPIO_PIN_3); //PF2-PF3
GPIOPinConfigure(GPIO_PF2_M1PWM6); //PF2[M1PWM6]
GPIOPinConfigure(GPIO_PF3_M1PWM7); //PF3[M1PWM7]

freq = (SysCtlClockGet()/40000); //40kHz switching

      //-----PWM Module0-----//
PWMGenConfigure(PWM0_BASE, PWM_GEN_0, PWM_GEN_MODE_DOWN); //GEN0_M0
PWMGenPeriodSet(PWM0_BASE, PWM_GEN_0, freq); //GEN0_M0PWM0-M0PWM1_50Hz
PWMPulseWidthSet(PWM0_BASE, PWM_OUT_0, freq*Dr); //M0PWM0, Duty
PWMPulseWidthSet(PWM0_BASE, PWM_OUT_1, freq*Dr); //M0PWM1, Duty
PWMOutputInvert(PWM0_BASE, PWM_OUT_1_BIT, true); //M0PWM1
PWMOutputState(PWM0_BASE, PWM_OUT_0_BIT, true); //M0PWM0
PWMOutputState(PWM0_BASE, PWM_OUT_1_BIT, true); //M0PWM1

PWMGenConfigure(PWM0_BASE, PWM_GEN_3, PWM_GEN_MODE_DOWN); //GEN3_M0
PWMGenPeriodSet(PWM0_BASE, PWM_GEN_3, freq); //GEN3_M0PWM6-M0PWM7_50Hz
PWMPulseWidthSet(PWM0_BASE, PWM_OUT_6, freq*Dr); //M0PWM6, Duty
PWMPulseWidthSet(PWM0_BASE, PWM_OUT_7, freq*Dr); //M0PWM7, Duty
PWMOutputInvert(PWM0_BASE, PWM_OUT_6_BIT, true); //M0PWM6
PWMOutputState(PWM0_BASE, PWM_OUT_6_BIT, true); //M0PWM6
PWMOutputState(PWM0_BASE, PWM_OUT_7_BIT, true); //M0PWM6

      //-----PWM Module1-----//
PWMGenConfigure(PWM1_BASE, PWM_GEN_1, PWM_GEN_MODE_DOWN); //GEN1_M1
PWMGenPeriodSet(PWM1_BASE, PWM_GEN_1, freq); //GEN1_M1PWM2-M1PWM3_40kHz
PWMPulseWidthSet(PWM1_BASE, PWM_OUT_2, freq*Dll/1000); //M1PWM2, Duty
PWMPulseWidthSet(PWM1_BASE, PWM_OUT_3, freq*Dll/1000); //M1PWM3, Duty
PWMOutputInvert(PWM1_BASE, PWM_OUT_2_BIT, true); //M1PWM2
PWMOutputState(PWM1_BASE, PWM_OUT_2_BIT, true); //M1PWM2
PWMOutputState(PWM1_BASE, PWM_OUT_3_BIT, true); //M1PWM3


PWMGenConfigure(PWM1_BASE, PWM_GEN_3, PWM_GEN_MODE_DOWN); //GEN3_M1
PWMGenPeriodSet(PWM1_BASE, PWM_GEN_3, freq); //GEN3_M1PWM6-M1PWM7_40kHz
PWMPulseWidthSet(PWM1_BASE, PWM_OUT_6, freq*Dlr/1000); //M1PWM6, Duty
```

```
	PWMPulseWidthSet(PWM1_BASE, PWM_OUT_7, freq*Dlr/1000); //M1PWM7, Duty
	PWMOutputInvert(PWM1_BASE, PWM_OUT_6_BIT, true); //M1PWM6
	PWMOutputState(PWM1_BASE, PWM_OUT_6_BIT, true); //M1PWM6
	PWMOutputState(PWM1_BASE, PWM_OUT_7_BIT, true); //M1PWM7

		//-----PWM Interrupt-----//
	PWMIntEnable(PWM1_BASE, PWM_INT_GEN_1);
	PWMGenIntTrigEnable(PWM1_BASE, PWM_GEN_1, PWM_INT_CNT_ZERO);
	IntEnable(INT_PWM1_1);
	IntPrioritySet(INT_PWM1_1, 1); //Highest(0)-->Lowest(224)

	PWMGenEnable(PWM0_BASE, PWM_GEN_0); //M0_GEN0
	PWMGenEnable(PWM0_BASE, PWM_GEN_3); //M0_GEN3
	PWMGenEnable(PWM1_BASE, PWM_GEN_1); //M1_GEN1
	PWMGenEnable(PWM1_BASE, PWM_GEN_3); //M1_GEN3
	//=====PWM setup [end]=====//

	//=====GPIO Interrupt [start]=====//
	GPIOPinTypeGPIOInput(GPIO_PORTB_BASE, GPIO_PIN_4); //PB4
	GPIOIntTypeSet(GPIO_PORTB_BASE, GPIO_PIN_4, GPIO_FALLING_EDGE); //PB4
	GPIOIntEnable(GPIO_PORTB_BASE, GPIO_PIN_4); //PB4
	IntEnable(INT_GPIOB); //Port B
	IntPrioritySet(INT_GPIOB, 0); //Highest(0)-->Lowest(224)
	//=====GPIO Interrupt [end]=====//

	IntMasterEnable();
	while(1)
	{}
}
//********************Main Code [end]********************//

//********************PWM1-GEN1 Interrupt [start]********************//
void PWM1GEN1_Int() {
	PWMGenIntClear(PWM1_BASE, PWM_GEN_1, PWM_INT_CNT_ZERO);

	ma = 0.9;
	if ((period < 796) || (period > 804)) {
		halfadd = 0;
	}
	else {
		halfadd = period/2 - 400; //halfadd <= |2|
	}

	if (period_count < 808) {period_count++;}
	else {}

	if (delay < 320) {delay++;} //320*0.025ms=8ms
	else if (delay == 320) {i = 678; delay++;}
	else {}

	if (i <= (200 + halfadd)) {
		ll = (i%2 == 0)?i:0;
		lr = (i%2 == 0)?0:i;
		Dll = 1000 - ma*Dsin[ll];
		Dlr = 1000 - ma*Dsin[lr];
		i++;
	}
```

```
        else if (i <= (399 + halfadd)) {
                ll = (i%2 == 0)?(400 + halfadd - i):0;
                lr = (i%2 == 0)?0:(400 + halfadd - i);
                Dll = 1000 - ma*Dsin[ll];
                Dlr = 1000 - ma*Dsin[lr];
                i++;
        }
        else if (i < 405) {
                Dll = 1000;
                Dlr = 1000;
                Dr = 1 - Dr;
                i = 1;
        }
        else {
                Dll = 1000;
                Dlr = 1000;
                Dr = 0;
                i = 1;
        }
        PWMOutputState(PWM0_BASE, PWM_OUT_0_BIT, Dr); //M0PWM0
        PWMOutputState(PWM0_BASE, PWM_OUT_1_BIT, Dr); //M0PWM1
        PWMOutputState(PWM0_BASE, PWM_OUT_6_BIT, Dr); //M0PWM6
        PWMOutputState(PWM0_BASE, PWM_OUT_7_BIT, Dr); //M0PWM7

        PWMPulseWidthSet(PWM1_BASE, PWM_OUT_2, freq*Dll/1000); //M1PWM2, Duty
        PWMPulseWidthSet(PWM1_BASE, PWM_OUT_3, freq*Dll/1000); //M1PWM3, Duty
        PWMPulseWidthSet(PWM1_BASE, PWM_OUT_6, freq*Dlr/1000); //M1PWM6, Duty
        PWMPulseWidthSet(PWM1_BASE, PWM_OUT_7, freq*Dlr/1000); //M1PWM7, Duty
}
//********************PWM1-GEN1 Interrupt [end]********************//

//********************GPIOB Interrupt [start]********************//
void GPIOB_Int(void) {
        GPIOIntClear(GPIO_PORTB_BASE, GPIO_INT_PIN_4); //Clear the GPIO interrupt

        period = period_count;
        period_count = 0;
        delay = 0;
}
//********************GPIOB Interrupt [end]********************//
```

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